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VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
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declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the above-identified Japanese Application from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese Application to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereof.

September 4, 2008
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【Name of Article】	Drawings	1
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[TITLE OF THE INVENTION] Semiconductor Device and Manufacturing Method of Semiconductor Device

[SCOPE OF CLAIM FOR PATENT]

[Claim 1] A manufacturing method of a semiconductor device having the steps of:

forming a metal connection exposing its upper surface in a groove section of an insulating film formed on a semiconductor substrate;

diffusing silicon into said metal connection from its upper surface; and

forming a metal diffusion preventing film on an exposed surface of said metal connection.

[Claim 2] A manufacturing method of a semiconductor device having the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming second and third insulating films sequentially on said first metal diffusion preventing film;

forming an opening through said first metal diffusion preventing film, said second insulating film and said third insulating film to expose the upper surface of said first metal connection;

forming a first groove section in said third insulating layer and leading to said opening;

burying a metal in said opening and said first groove section to form a via plug connecting a second metal connection

in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[Claim 3] A manufacturing method of a semiconductor device having the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming second and third insulating films sequentially on said first metal diffusion preventing film;

selectively etching said third insulating film to form a first groove section;

forming an opening through said first metal diffusion preventing film, said second insulating film and said third insulating film and leading to said first groove section to expose the upper surface of said first metal connection;

burying a metal in said opening and said first groove section and said opening to form a via plug connecting a second metal connection in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[Claim 4] A manufacturing method of a semiconductor device having the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming a second insulating film and an etching stopper film sequentially on said first metal diffusion preventing film;

selectively etching said etching stopper film to form a first opening exposing said second insulating film;

forming a third insulating film on an exposed surface of said second insulating film and said etching stopper film;

forming a first groove section leading to said first opening and having a larger width than that of said first opening, in said third insulating film;

forming a second opening through said first metal diffusion preventing film, said second insulating film and said third insulating film at a position including said first opening to expose said first metal connection;

burying a metal in said first groove section said first opening and said second opening to form a via plug connecting a second metal connection in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[Claim 5] A manufacturing method of a semiconductor device having the steps of:

forming a first metal connection exposing its upper

surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming a second insulating film on said first metal diffusion preventing film;

forming an opening in said metal diffusion preventing film and said second insulating film to expose said first metal connection;

burying metal in said opening to form a via plug;

forming a third insulating film covering an exposed surface of said via plug and said second insulating film;

selectively etching said third insulating film to expose said second insulating film and form a first groove section leading to said via plug;

burying a metal in said first groove section to form a second metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[Claim 6] The manufacturing method as set forth in claim 5, wherein silicon is diffused into said via plug.

[Claim 7] A manufacturing method of a semiconductor device having a first metal connection formed in a groove section of an insulating film formed on a semiconductor substrate, a second metal connection provided on a second insulating film covering said first metal connection, and a via plug for connecting said first metal connection to said second metal connection, having the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

forming a second insulating film on an exposed surface of said first metal connection and said first insulating film;

selectively etching said second insulating film to expose said first metal connection, to thereby form an opening;

burying metal in said opening to form said via plug;

diffusing silicon from the upper surface of said via plug; and

forming said metal connection covering an exposed surface of said via plug.

[Claim 8] The manufacturing method of a semiconductor device as set forth in claim 1, wherein silicon is diffused into the entire connection of said metal connection.

[Claim 9] The manufacturing method of a semiconductor device as set forth in claim 8, wherein a silicon concentration of said metal connection is maximum at its upper surface.

[Claim 10] The manufacturing method of a semiconductor device as set forth in claim 8 or 9, wherein a silicon concentration of said metal connection is not larger than 8 atoms %.

[Claim 11] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein silicon is diffused into the entire connection of said first metal connection.

[Claim 12] The manufacturing method of a semiconductor device as set forth in claim 11, wherein a silicon concentration of said first metal connection is maximum at its upper surface.

[Claim 13] The manufacturing method of a semiconductor device as set forth in claim 11 or 12, wherein a silicon

concentration of said first metal connection is not larger than 8 atoms %.

[Claim 14] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein silicon is diffused into the entire connection of said second metal connection.

[Claim 15] The manufacturing method of a semiconductor device as set forth in claim 14, wherein a silicon concentration of said second metal connection is maximum at its upper surface.

[Claim 16] The manufacturing method of a semiconductor device as set forth in claim 14 or 15, wherein a silicon concentration of said second metal connection is not larger than 8 atoms %.

[Claim 17] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 18] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 19] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 20] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said first insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 21] The manufacturing method of a semiconductor

device as set forth in one of claims 2 to 5 and 7, wherein said first insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 22] The manufacturing method of a semiconductor device as set forth in one of claim 2 to 5 and 7, wherein said first insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 23] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein said third insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 24] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein said third insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 25] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein said third insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 26] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 27] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein said first metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 28] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein said second metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 29] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said second insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 30] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said second insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 31] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said second insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 32] The manufacturing method of a semiconductor device as set forth in one of claims 18, 19, 21, 22, 24, 25, 30 and 31, wherein said ladder-type hydrogen siloxane is L-Ox.

[Claim 33] The manufacturing method of a semiconductor device as set forth in one of claims 18, 19, 21, 22, 24, 25, 30 and 31, wherein said ladder-type hydrogen siloxane has a film density of not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3.

[Claim 34] The manufacturing method of a semiconductor device as set forth in one of claims 18, 19, 21, 22, 24, 25, 30 and 31, wherein said ladder-type hydrogen siloxane has a film refractive index of not smaller than 1.38 nm and not larger than 1.40 nm at a wavelength of 633 nm.

[Claim 35] The manufacturing method of a semiconductor

device as set forth in claim 1, wherein said second insulating film has an etching stopper film.

[Claim 36] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said etching stopper film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 37] The manufacturing method of a semiconductor device as set forth in claim 1, wherein after the step of forming said metal connection in the groove section of said insulating film, a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen is removed, and, after said metal oxide layer is removed, silicon is diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[Claim 38] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of forming said first metal connection in the groove section of said first insulating film, a metal oxide layer formed by exposing the upper surface of said first metal connection to oxygen is removed, and, after said metal oxide layer is removed, silicon is diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[Claim 39] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of burying the metal in the groove section of said second metal connection, a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen is removed, and, after said metal oxide layer is removed, silicon is diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[Claim 40] The manufacturing method of a semiconductor

device as set forth in claim 1, wherein after the step of forming said metal connection in the groove section of said insulating film, an oxidation preventing layer is formed on a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen, said metal oxide layer and said oxidation preventing layer are removed in a closed processing chamber, and, silicon is diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[Claim 41] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of forming said first metal connection in the groove section of said first insulating film, an oxidation preventing layer is formed on a metal oxide layer formed by exposing the upper surface of said first metal connection to oxygen, said metal oxide layer and said oxidation preventing layer are removed in a closed processing chamber, and, silicon is diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[Claim 42] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of burying the metal in the groove section of said second metal connection, an oxidation preventing layer is formed on a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen, said metal oxide layer and said oxidation preventing layer are removed in a closed chamber, and, silicon is diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[Claim 43] The manufacturing method of a semiconductor device as set forth in claim 1, wherein after the step of forming said metal connection in the groove section of said

insulating film, a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen is removed, said oxidation preventing layer is removed by heating it in a closed processing chamber, and, silicon is diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[Claim 44] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of forming said first metal connection in the groove section of said first insulating film, a metal oxide layer formed by exposing the upper surface of said first metal connection to oxygen is removed, said oxidation preventing layer is removed by heating it in a closed processing chamber, and, silicon is diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[Claim 45] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5, wherein after the step of burying the metal in the groove section of said second metal connection, a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen is removed, said oxidation preventing layer is removed by heating it in a closed chamber, and, silicon is diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[Claim 46] The manufacturing method of a semiconductor device as set forth in one of claims 1 to 7 and 37 to 45, wherein at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas is used at the step of diffusing silicon.

[Claim 47] The manufacturing method of a semiconductor device as set forth in one of claims 37 to 42, wherein a reducing operation gas is used for removing the metal oxide

layer.

[Claim 48] The manufacturing method of a semiconductor device as set forth in claim 47, wherein said reducing operation gas includes at least one of H_2, He, N_2 and NH_3.

[Claim 49] The manufacturing method of a semiconductor device as set forth in one of claims 40 to 45, wherein said oxidation preventing layer is a film including at least one of benzotriazole and benzotriazole derivative.

[Claim 50] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said metal connection includes at least one of copper and copper alloy.

[Claim 51] The manufacturing method of a semiconductor device as set forth in claim 1, wherein said metal connection has a barrier metal.

[Claim 52] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said first metal connection includes at least one of copper and copper alloy.

[Claim 53] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said first metal connection has a barrier metal.

[Claim 54] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said second metal connection includes at least one of copper and copper alloy.

[Claim 55] The manufacturing method of a semiconductor device as set forth in one of claims 2 to 5 and 7, wherein said second metal connection has a barrier metal.

[Claim 56] The manufacturing method of a semiconductor device as set forth in one of claims 50, 52 and 54, wherein said copper alloy includes at least one of Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

[Claim 57] The manufacturing method of a semiconductor

device as set forth in one of claims 51, 53 and 55, wherein said barrier metal has at least one of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

[Claim 58] A semiconductor device having:

a first metal connection provided in a groove section in a first insulating film formed on a semiconductor substrate, silicon being diffused into said first metal connection; and

a metal diffusion preventing film covering an exposed surface of said first metal connection.

[Claim 59] The semiconductor device as set forth in claim 58, having:

a via plug connected to an upper surface of said first metal connection and provided in said first metal diffusion preventing film and a second insulating film formed on said first metal diffusion preventing film;

a second metal connection connected to said via plug and provided in a third insulating film formed on said second insulating film, silicon being diffused into said second metal connection; and

a second metal diffusion preventing film covering an exposed surface of said second metal connection.

[Claim 60] The semiconductor device as set forth in claim 59, having a barrier metal provided between said via plug and said second metal connection for separating said via plug from said second metal connection.

[Claim 61] The semiconductor device as set forth in claim 59 or 60, wherein silicon is diffused into said via plug.

[Claim 62] A semiconductor device having:

a first metal connection provided in a groove section in a first insulating film formed on a semiconductor substrate;

a metal diffusion preventing film covering a via plug connected to an upper surface of said first metal connection

and provided in said first metal diffusion preventing film and a second insulating film formed on said first metal diffusion preventing film, silicon being diffused into said via plug; and

a second metal connection connected to said via plug and provided in a third insulating film formed on said second insulating film, silicon being diffused into said second metal connection.

[Claim 63] The semiconductor device as set forth in claim 62, wherein said via plug is integral with said second metal connection.

[Claim 64] The semiconductor device as set forth in claim 62 or 63, wherein silicon is diffused into the entirety of said via plug.

[Claim 65] The semiconductor device as set forth in claim 64, wherein a silicon concentration of said via plug is maximum at its upper surface.

[Claim 66] The semiconductor device as set forth in claim 64 or 65, wherein a silicon concentration of said via plug is not larger than 8 atoms %.

[Claim 67] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein silicon is diffused into the entire connection of said first metal connection.

[Claim 68] The semiconductor device as set forth in claim 67, wherein a silicon concentration of said first metal connection is maximum at its upper surface.

[Claim 69] The semiconductor device as set forth in claim 67 or 68, wherein a silicon concentration of said first metal connection is not larger than 8 atoms %.

[Claim 70] The semiconductor device as set forth in one of claim 59 or 62, wherein silicon is diffused into the entire connection of said second metal connection.

[Claim 71] The semiconductor device as set forth in

claim 70, wherein a silicon concentration of said second metal connection is maximum at its upper surface.

[Claim 72] The semiconductor device as set forth in claim 70 or 71, wherein a silicon concentration of said second metal connection is not larger than 8 atoms %.

[Claim 73] The semiconductor device as set forth in claim 58 or 59, wherein said first metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 74] The manufacturing method of a semiconductor device as set forth in claim 59, wherein said second metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film.

[Claim 75] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein said first insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 76] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein said first insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 77] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein said insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 78] The semiconductor device as set forth in claim 59 or 62, wherein said second insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 79] The semiconductor device as set forth in claim 59 or 62, wherein said second insulating film includes at least one of a ladder-type hydrogen siloxane and a porous

ladder-type hydrogen siloxane.

[Claim 80] The semiconductor device as set forth in claim 59 or 62, wherein said second insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 81] The semiconductor device as set forth in claim 59 or 62, wherein said third insulating film includes at least one of SiO_2, SiOC and an organic film.

[Claim 82] The semiconductor device as set forth in claim 59 or 62, wherein said third insulating film includes at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[Claim 83] The semiconductor device as set forth in claim 59 or 62, wherein said third insulating film has a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film having at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film having SiO_2.

[Claim 84] The semiconductor device as set forth in claims 76, 77, 79, 80, 82 and 83, wherein said ladder-type hydrogen siloxane is L-Ox.

[Claim 85] The semiconductor device as set forth in one of claims 76, 77, 79, 80, 82 and 83, wherein said ladder-type hydrogen siloxane has a film density of not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3.

[Claim 86] The semiconductor device as set forth in one of claims 76, 77, 79, 80, 82 and 83, wherein said ladder-type hydrogen siloxane has a film refractive index of not smaller than 1.38 nm and not larger than 1.40 nm at a wavelength of

633 nm.

[Claim 87] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein said first metal connection includes at least one of copper and copper alloy.

[Claim 88] The semiconductor device as set forth in one of claims 58, 59 and 62, wherein said first metal connection has a barrier metal.

[Claim 89] The semiconductor device as set forth in claim 58, 59 and 62, wherein said second metal connection and said via plug include at least one of copper and copper alloy.

[Claim 90] The semiconductor device as set forth in claim 59 or 62, wherein said second metal connection and said via plug have barrier metals.

[Claim 91] The semiconductor device as set forth in claim 87 or 89, wherein said copper alloy includes at least one of Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

[Claim 92] The semiconductor device as set forth in claim 88 or 90, wherein said barrier metal has at least one of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a semiconductor device having metal connections such as Cu connections, and its manufacturing method.

[0002]

[Prior Art]

In a manufacturing field of semiconductor devices, as the operational speed and integration of devices have been enhanced, the device design rule has been reduced. As the devices have been reduced, the connection size and the connection spacing have also been reduced, so that the

resistance of connections and the inter-connection parasitic capacitance have a tendency to be increased. When the resistance of connections and the inter-connection parasitic capacitance have been increased, the time constant has been increased to delay the propagation of signals on the connections, which would be a problem in terms of increasing the operation speed of devices.

[0003]

As a result, as a method for decreasing the connection resistance, technology and products using Cu (copper) having a lower specific resistance than Al (aluminum) as connection material have been prevailed. When Cu is used as connection material, since it is difficult to subject Cu to a fine-formation by a dry etching, a groove connection called a damascene connection formed by using a CMP (chemical mechanical polishing) process is generally and broadly used.

[0004]

Fig. 34 is a cross-sectional view illustrating a structure of a prior art groove connection.

[0005]

As illustrated in Fig. 34, in a groove connection, a barrier metal 105 for preventing Cu from being diffused is formed within a groove of a SiO_2 insulating film 102 grown on an underlying insulating film 101 formed on a semiconductor substrate (not shown), and a Cu connection 107 whose bottom surface and side faces are covered by the barrier metal 105 is formed. In the shown structure, a SiN film 112 on the Cu connection 107 and a SiO_2 interlayer insulating film 110 for securing insulating characteristics of the Cu connection 107 from an upper connection (not shown) are sequentially formed.

[0006]

In a forming process for the shown structure, after the formation of the groove connection, when the SiO_2 interlayer

insulating film 110 is formed on the Cu connection 107, Cu easily reacts with SiO_2, so that Cu is diffused into the SiO_2 film. Therefore, the SiN film 112 whose thickness is about 50 to 150 nm is grown by a plasma CVD method on the Cu connection 107, and after that, the SiO_2 interlayer insulating film 110 is grown.

[0007]

By the way, as Cu serving as connection material has been prevailed, the improvement of the anti-electromigration characteristic of the Cu connection has been required, a structure and method for enhancing the anti-oxidation characteristic of the periphery of the Cu connection are disclosed as a method for the above-improvement in a document (for example, refer to non-patent document 1). This document suggests that, while a Si substrate having a Cu connection is heated, the Si substrate is exposed in a SiH_4 gas atmosphere, so that the Cu connection reacts with Si (silicon) in the SiH_4 gas. As a result, a Cu silicide layer is formed on the surface of the Cu connection, thus improving the anti-electromigration characteristic of the Cu connection.

[0008]

When a SiN film is grown as a Cu diffusion preventing film on the Cu connection, a Cu silicide layer is first formed by using SiH_4 gas as a reactive growing gas, and the SiN film is grown thereon, to improve the electromigration (ZM) of the Cu connection.

[0009]

Recently, in order to decrease the inter-connection parasitic capacitance, a SiC film or a SiCN film having a lower specific resistance than that of the SiN film 112 is considered. Also, in recent years, in order to decrease the cost and decrease the resistance of a via serving as a connection hole, a dual damascene-structured connection simultaneously

burying vias and connections is considered.

[0010]

The following three methods are now known for forming dual damascene-structured connections. A first method is to form an insulating film between different layers for insulating connections formed by different layers from each other and an inter-connection insulating film for insulating the connections having the same layer from each other are grown. Then, an etching of an via is first carried out and then, a groove connection is formed, thus forming the via and connection. This is called a via first method (hereinafter, referred to as a VF method). A second method is to grow an insulating film between different layers. Then, a mask insulating film for a via etching is grown on the insulating film and is etched to obtain a via pattern. Then, an inter-connection insulating film is grown. When etching a connection groove, an etching of a via is carried out simultaneously with etching of the connection through the mask insulating film for via etching. This is called a middle first method (hereinafter, referred to as an MF method). A third method is to grow an insulating film between different layers and an inter-connection insulating film. Then, etching is carried out to form a connection groove, and then, a via is formed, thus forming a via and a connection. This is called a trench first method (hereinafter, referred to as a TF method).

[0011]

At the present time, mainly in view of photoresist steps, the VF method is used for forming a lower connection portion having a fine connection structure, while the TF method or the MF method is used for forming an upper connection layer where the connection width and the via diameter are relatively large.

[0012]

[Non-patent document 1]

The Institute of Electronics, Information and Communication Engineers, 1995, Electronics Science Proceeding 2, C-418, pp.115-116.

[0013]

[Problems to be Solved by the Invention]

Problems on the prior art groove connection structure using the above-mentioned SiC film or SiCN film as a Cu diffusion preventing film will be explained.

[0014]

1. When growing a SiN film as a Cu diffusion preventing film on a Cu connection, SiH_4, NH_3 and N_2 are generally used as reaction gas for growing by a CVD method. Therefore, when growing the SiN film, SiH_4 gas, NH_3 gas and N_2 gas are introduced into a film growing processing chamber of a CVD apparatus, while the temperature of a semiconductor substrate on which a Cu connection is formed and the pressure within the processing chamber are being stabilized, a Cu silicide layer is formed by the SiH_4 gas on the Cu connection, thus improving the anti-electromigration characteristic.

[0015]

However, when growing a SiC film or a SiCN film as a Cu diffusion preventing film on a Cu connection, organic silane gas such as $SiH(CH_3)_3$ or $Si(CH_3)_4$ is broadly used as reaction gas, so that SiH_4 is not used. In a Si compound gas including these organic groups, since the binding energy between Si and an organic group is larger than the binding energy between Si and H, so that thermal decomposition is easier in the Si compound gas than in SiH_4. As a result, even if the Cu connection is exposed to a gas atmosphere of $SiH(CH_3)_3$ or $Si(CH_3)_4$, a reaction between Cu and Si is lower than as compared with a case where the Cu connection is exposed to a gas

atmosphere of SiH_4. Therefore, when growing a SiC film or a SiCN film on a Cu connection, a Cu silicide layer by a growing reaction gas is hardly formed on the surface of Cu as compared with a case where a SiC film is grown.

[0016]

Also, when a Cu silicide layer is not formed on the surface of the Cu connection, a contact characteristic between the Cu connection and SiC film or the SiCN film deteriorates, so that a Cu crystal grain in the Cu connection can not be stabilized, which would invite deterioration of the anti-electromigration characteristic of the Cu connection. Further, the anti-stress characteristic would deteriorate, and the Cu connection would be easily disconnected by a stress or the like of a protection film formed on the upper layer.

[0017]

2. Since the specific resistance of the Cu silicide layer is higher than that of Cu, the connection resistance becomes larger, which is a problem. Also, since the Cu silicide layer is formed only on the uppermost surface of the Cu connection, when a connection hole is perforated for an upper connection layer, the Cu silicide layer is removed by etching the connection hole. Therefore, in order to improve the electromigration and the stress migration, the Cu silicide layer has to be sufficiently thicker. Therefore, the connection resistance becomes much larger, which is a problem.

[0018]

3. When forming a Cu silicide layer by exposing a Si connection to the SiH_4 gas atmosphere, when the surface of the Cu is oxidized to form a Cu oxide layer, the Cu oxide layer on the surface reacts with Si, to abnormally grow mixture of Cu, Si and O. This abnormal growth does not only increase the connection resistance, but also a large amount of such mixture would be generated at an interface between Cu at the upper

surface of the Cu connection and the barrier metal, so that connections are easily short-circuited where the spacing is small. This is a problem.

[0019]

4. As a Cu corrosion preventing method, it is generally known that a Cu oxide layer reacts with BTA (benzotriazole) to form a BTA layer on the surface of Cu to stop the process of oxidation. As a result, after the Cu connection is formed, a corrosion processing step is added to avoid oxidation of Cu. However, if the BTA layer remains, since reaction between Si and SiH_4 is also suppressed, a step for removing the BTA layer is required. Also, even if the step for removing the BTA layer is introduced, when the Cu connection is exposed to the air after the BTA layer is removed, oxygen in the air reacts with Cu, so that a Cu oxide layer is formed on the surface of the Cu connection, the Cu oxide layer causing the abnormal growth.

[0020]

Next, a problem occurred when a damascene structure is formed will be explained.

[0021]

5. First, a dual damascene forming method by the VF method is explained briefly. Fig. 35 to Fig. 37 are cross-sectional views illustrating double-layered connections by a dual damascene forming method using the VF method

[0022]

First, after a first copper connection 330 is formed, a Cu diffusion preventing film SiCN film 311, a SiO_2 film 312 serving as an insulating film between different layers, a SiCN film 313 serving as an etching stopper film, and a SiO_2 film 317 serving as a second insulating film between different layers are grown, and a photoresist step of a via section is first carried out (Fig. 35(a)). Next, an etching is carried out to reach the SiCN film 311 serving as the diffusion

preventing film provided on the first copper connection 330, and the photoresist 314 of vias is removed by an O_2 dry etching and wet stripping and the like (Fig. 35(b)). Then, a reflection preventing film 25 is buried in vias, and a photoresist step for a second groove connection is carried out (Fig. 36(c)), so that the second groove connection is etched. After that, the photoresist of the second groove connection is removed by an O_2 dry etching and a wet stripping and the like (Fig. 36(d)). Subsequently, the SiCN film 311 on the first copper connection 330 is removed by an etching back to form a connection hole to the lower connection (Fig. 36(e)). Then, a stacked film by forming tantalum (Ta) on tantalum nitride (TaN) (hereinafter, represented by Ta/TaN film), and a Cu film 321 are buried in a via and a groove for a second groove connection (Fig. 37(f)), and the Ta/TaN film and the Cu film 321 on the SiO_2 film 317 are removed by a CMP method to form a second copper connection 332, and then, a SiCN film 322 is formed (Fig. 37(g)).

[0023]

In case of the VF method, as illustrated in Fig. 35(b), etching is carried out to reach the SiCN film 311 serving as a diffusion preventing film at a via etching step; however, in view of the opening diameter and opening ratio of vias and the etching selection ratio, it is difficult to stop the etching by the SiCN film 311 at all vias. As a result, at a via where the SiCN film 311 serving as a diffusion preventing film is removed at a via etching, the copper connection at the via bottom is exposed by the O_2 dry etching and wet stripping liquid by the etching of the via and the second groove connection, so that the surface of the copper connection is oxidized and eroded to form an oxide layer 331 of copper, thus decreasing the manufacturing yield of vias and the reliability represented by the via EM.

[0024]

Further, when a rework or recommence due to the dimension deviation and position deviation at the photolithography steps of the second groove connection is carried out, the copper connection at the via bottom is exposed to the O_2 dry ashing and the wet stripping liquid every rework, so that the oxidation and erosion of the copper surface are further enhanced.

[0025]

Here, a relationship between the number of reworks at the photolithography step of the second groove connection and the via chain manufacturing yield is explained.

[0026]

Fig. 38 is a graph showing a result evaluating the via chain manufacturing yield. Note that via chains used in this evaluation is for calculating a defective ratio of vias and are constructed so that their resistance values can be measured. When a measured resistance value is deviated from a predetermined standard, a via having such a resistance value is determined to be defective.

[0027]

As illustrated in Fig. 38, when the number of reworks is increased, the via chain manufacturing yield is decreased by the oxidation and erosion of the copper surface within the vias. This means that rework at the photolithography step invites deterioration of the reliability represented by the via EM. This problem occurs in all the damascene connection forming methods as well as the VF method when insulating films above a Cu connection are etched.

[0028]

6. Usually, when an interlayer insulating film grown on a copper connection is etched, there is a problem of interference by reflection from the lower copper connection occurred when a photoresist is exposed by light at a

photolithography process. Therefore, in order to suppress the reflection from the copper connection, a reflection preventing film is grown before the photoresist is coated. However, when a dual damascene connection is formed, in the MF method, when the reflection preventing film is removed, its underlying insulating film is subject to etching damage, so that a reflection preventing film can not be used at a photolithography step for forming a mask insulating film at a via etching and for an upper groove connection. Also, in the TF method, when an insulating film below a formed connection groove is etched, if a reflection preventing is buried in the connection groove, it is impossible to etch the insulating film, and thus, a reflection preventing film can not be used at a photolithography step of a via.

[0029]

The present invention is to solve the above-mentioned problems the prior art has, and its object is to provide a semiconductor device and its manufacturing method which improves the contact characteristics between a metal connection such as a Cu connection and a metal diffusion preventing film, increases the life time of a metal connection by improving the anti-electromigration characteristics of the metal connection and suppresses the increase of the connection resistance.

[0030]

[Means for solving the Problems]

In order to achieve the above-mentioned object, a manufacturing method of a semiconductor device according to the present invention has the steps of:

forming a metal connection exposing its upper surface in a groove section of an insulating film formed on a semiconductor substrate;

diffusing silicon into said metal connection from its

upper surface; and

forming a metal diffusion preventing film on an exposed surface of said metal connection.

[0031]

Also, a manufacturing method of a semiconductor device according to the present invention has the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming second and third insulating films sequentially on said first metal diffusion preventing film;

forming an opening through said first metal diffusion preventing film, said second insulating film and said third insulating film to expose the upper surface of said first metal connection;

forming a first groove section in said third insulating layer and leading to said opening;

burying a metal in said opening and said first groove section to form a via plug connecting a second metal connection in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[0032]

Also, a manufacturing method of a semiconductor device according to the present invention has the steps of:

forming a first metal connection exposing its upper

surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first insulating film;

forming second and third insulating films sequentially on said first metal diffusion preventing film;

selectively etching said third insulating film to form a first groove section;

forming an opening through said first metal diffusion preventing film, said second insulating film and said third insulating film and leading to said first groove section to expose the upper surface of said first metal connection;

burying a metal in said opening and said first groove section and said opening to form a via plug connecting a second metal connection in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[0033]

Also, a manufacturing method of a semiconductor device according to the present invention has the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first

insulating film;

forming a second insulating film and an etching stopper film sequentially on said first metal diffusion preventing film;

selectively etching said etching stopper film to form a first opening exposing said second insulating film;

forming a third insulating film on an exposed surface of said second insulating film and said etching stopper film;

forming a first groove section leading to said first opening and having a larger width than that of said first opening, in said third insulating film;

forming a second opening through said first metal diffusion preventing film, said second insulating film and said third insulating film at a position including said first opening to expose said first metal connection;

burying a metal in said first groove section said first opening and said second opening to form a via plug connecting a second metal connection in said first groove section to said first metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[0034]

Also, a manufacturing method of a semiconductor device according to the present invention has the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

diffusing silicon into said first metal connection from its upper surface;

forming a first metal diffusion preventing film on an exposed surface of said first metal connection and said first

insulating film;

forming a second insulating film on said first metal diffusion preventing film;

forming an opening in said metal diffusion preventing film and said second insulating film to expose said first metal connection;

burying metal in said opening to form a via plug;

forming a third insulating film covering an exposed surface of said via plug and said second insulating film;

selectively etching said third insulating film to expose said second insulating film and form a first groove section leading to said via plug;

burying a metal in said first groove section to form a second metal connection;

diffusing silicon into said second metal connection from its upper surface; and

forming a second metal diffusion preventing film on an exposed surface of said second metal connection.

[0035]

In this case, silicon may be diffused into said via plug.

[0036]

Also, a manufacturing method of a semiconductor device according to the present invention has a first metal connection formed in a groove section of an insulating film formed on a semiconductor substrate, a second metal connection provided on a second insulating film covering said first metal connection, and a via plug for connecting said first metal connection to said second metal connection, has the steps of:

forming a first metal connection exposing its upper surface in a groove section of a first insulating film formed on a semiconductor substrate;

forming a second insulating film on an exposed surface of said first metal connection and said first insulating film;

selectively etching said second insulating film to expose said first metal connection, to thereby form an opening;

burying metal in said opening to form said via plug;

diffusing silicon from the upper surface of said via plug; and

forming said metal connection covering an exposed surface of said via plug.

[0037]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, silicon may be diffused into the entire connection of said metal connection, a silicon concentration of said metal connection may be maximum at its upper surface, and a silicon concentration of said metal connection may not be larger than 8 atoms %.

[0038]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, silicon may be diffused into the entire connection of said first metal connection, a silicon concentration of said first metal connection may be maximum at its upper surface, and a silicon concentration of said first metal connection may not be larger than 8 atoms %.

[0039]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, silicon may be diffused into the entire connection of said second metal connection, a silicon concentration of said second metal connection may be maximum at its upper surface, and a silicon concentration of said second metal connection may be not larger than 8 atoms %.

[0040]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said insulating film may include at least one of SiO_2, SiOC and an organic film, and said insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0041]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0042]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said first insulating film may include at least one of SiO_2, SiOC and an organic film, and said first insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0043]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said first insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0044]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said third insulating film may include at least one of SiO_2, SiOC

and an organic film, and said third insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0045]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said third insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0046]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film, said first metal diffusion preventing film may include at least one of SiCN, SiC, SiOC and an organic film, and said second metal diffusion preventing film may include at least one of SiCN, SiC, SiOC and an organic film.

[0047]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said second insulating film may include at least one of SiO_2, SiOC and an organic film, and said second insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0048]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said second insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type

hydrogen siloxane and a porous ladder-type hydrogen siloxane, said upper film may have SiO_2.

[0049]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said ladder-type hydrogen siloxane may be L-Ox, said ladder-type hydrogen siloxane may have a film density of not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3, and said ladder-type hydrogen siloxane may have a film refractive index of not smaller than 1.38 nm and not larger than 1.40 nm at a wavelength of 633 nm.

[0050]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said second insulating film may have an etching stopper film. In this case, said etching stopper film may include at least one of SiCN, SiC, SiOC and an organic film.

[0051]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said metal connection in the groove section of said insulating film, a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen may be removed, and, after said metal oxide layer is removed, silicon may be diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[0052]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said first metal connection in the groove section of said first insulating film, a metal oxide layer formed by exposing the upper surface of said first metal

connection to oxygen may be removed, and, after said metal oxide layer is removed, silicon may be diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[0053]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of burying the metal in the groove section of said second metal connection, a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen may be removed, and, after said metal oxide layer is removed, silicon may be diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[0054]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said metal connection in the groove section of said insulating film, an oxidation preventing layer may be formed on a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen, said metal oxide layer and said oxidation preventing layer may be removed in a closed processing chamber, and, silicon may be diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[0055]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said first metal connection in the groove section of said first insulating film, an oxidation preventing layer may be formed on a metal oxide layer formed by exposing the upper surface of said first metal connection to oxygen, said metal oxide layer and said oxidation

preventing layer may be removed in a closed processing chamber, and, silicon may be diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[0056]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of burying the metal in the groove section of said second metal connection, an oxidation preventing layer may be formed on a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen, said metal oxide layer and said oxidation preventing layer may be removed in a closed chamber, and, silicon may be diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[0057]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said metal connection in the groove section of said insulating film, a metal oxide layer formed by exposing the upper surface of said metal connection to oxygen may be removed, said oxidation preventing layer is removed by heating it in a closed processing chamber, and, silicon may be diffused from the upper surface of said metal connection without exposing said metal connection layer to oxygen.

[0058]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of forming said first metal connection in the groove section of said first insulating film, a metal oxide layer formed by exposing the upper surface of said first metal

connection to oxygen may be removed, said oxidation preventing layer may be removed by heating it in a closed processing chamber, and, silicon may be diffused from the upper surface of said first metal connection without exposing said first metal connection layer to oxygen.

[0059]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, after the step of burying the metal in the groove section of said second metal connection, a metal oxide layer formed by exposing the upper surface of the metal connection buried in the groove section of said second metal connection to oxygen may be removed, said oxidation preventing layer may be removed by heating it in a closed chamber, and, silicon may be diffused from the upper surface of said metal without exposing said the surface of said metal to oxygen.

[0060]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, at least one of SiH_4 gas, Si_2H_6 gas and SiH_2Cl_2 gas may be used at the step of diffusing silicon.

[0061]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, a reducing operation gas may be used for removing the metal oxide layer. In this case, said reducing operation gas may include at least one of H_2, He, N_2 and NH_3. Also, said oxidation preventing layer may be a film including at least one of benzotriazole and benzotriazole derivative.

[0062]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said metal connection may include at least one of copper and copper

alloy, and said metal connection may have a barrier metal.

[0063]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said first metal connection includes at least one of copper and copper alloy, and said first metal connection may have a barrier metal.

[0064]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said second metal connection may include at least one of copper and copper alloy, and said second metal connection may have a barrier metal.

[0065]

Also, in the above-mentioned manufacturing method of a semiconductor device according to the present invention, said copper alloy may include at least one of Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe, and said barrier metal may have at least one of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

[0066]

In order to achieve the above-mentioned object, a semiconductor device according to the present invention has:

a first metal connection provided in a groove section in a first insulating film formed on a semiconductor substrate, silicon being diffused into said first metal connection; and

a metal diffusion preventing film covering an exposed surface of said first metal connection.

[0067]

Also, the above-mentioned semiconductor device according to the present invention may have:

a via plug connected to an upper surface of said first metal connection and provided in said first metal diffusion

preventing film and a second insulating film formed on said first metal diffusion preventing film;

a second metal connection connected to said via plug and provided in a third insulating film formed on said second insulating film, silicon being diffused into said second metal connection; and

a second metal diffusion preventing film covering an exposed surface of said second metal connection.

[0068]

In this case, a barrier metal may be provided between said via plug and said second metal connection for separating said via plug from said second metal connection, and silicon may be diffused into said via plug.

[0069]

A semiconductor device according to the present invention has:

a first metal connection provided in a groove section in a first insulating film formed on a semiconductor substrate;

a metal diffusion preventing film covering a via plug connected to an upper surface of said first metal connection and provided in said first metal diffusion preventing film and a second insulating film formed on said first metal diffusion preventing film, silicon being diffused into said via plug; and

a second metal connection connected to said via plug and provided in a third insulating film formed on said second insulating film, silicon being diffused into said second metal connection.

[0070]

In this case, said via plug may be integral with said second metal connection, silicon may be diffused into the entirety of said via plug, a silicon concentration of said via

plug may be maximum at its upper surface, and a silicon concentration of said via plug may not be larger than 8 atoms %.

[0071]

Also, in the above-mentioned semiconductor device according to the present invention, silicon may be diffused into the entire connection of said first metal connection, a silicon concentration of said first metal connection may be maximum at its upper surface, and a silicon concentration of said first metal connection may not be larger than 8 atoms %.

[0072]

Also, in the above-mentioned semiconductor device according to the present invention, silicon may be diffused into the entire connection of said second metal connection, a silicon concentration of said second metal connection may be maximum at its upper surface, and a silicon concentration of said second metal connection may not be larger than 8 atoms %.

[0073]

Also, in the above-mentioned semiconductor device according to the present invention, said first metal diffusion preventing film may include at least one of SiCN, SiC, SiOC and an organic film, and said second metal diffusion preventing film may include at least one of SiCN, SiC, SiOC and an organic film.

[0074]

Also, in the above-mentioned semiconductor device according to the present invention, said first insulating film may include at least one of SiO_2, SiOC and an organic film, and said first insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0075]

Also, in the above-mentioned semiconductor device

according to the present invention, said insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0076]

Also, in the above-mentioned semiconductor device according to the present invention, said second insulating film may include at least one of SiO_2, SiOC and an organic film, and said second insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0077]

Also, in the above-mentioned semiconductor device according to the present invention, said second insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0078]

Also, in the above-mentioned semiconductor device according to the present invention, said third insulating film includes at least one of SiO_2, SiOC and an organic film, and said third insulating film may include at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane.

[0079]

Also, in the above-mentioned semiconductor device according to the present invention, said third insulating film may have a stacked film formed by a lower film and an upper film formed on said lower film,

said lower film may have at least one of a ladder-type hydrogen siloxane and a porous ladder-type hydrogen siloxane,

said upper film may have SiO_2.

[0080]

Also, in the above-mentioned semiconductor device according to the present invention, said ladder-type hydrogen siloxane may be L-Ox, said ladder-type hydrogen siloxane has a film density of not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3, and said ladder-type hydrogen siloxane has a film refractive index of not smaller than 1.38 nm and not larger than 1.40 nm at a wavelength of 633 nm.

[0081]

Also, in the above-mentioned semiconductor device according to the present invention, said first metal connection may include at least one of copper and copper alloy, and said first metal connection may have a barrier metal.

[0082]

Also, in the above-mentioned semiconductor device according to the present invention, said second metal connection and said via plug may include at least one of copper and copper alloy, and said second metal connection and said via plug may have barrier metals.

[0083]

Further, in the above-mentioned semiconductor device according to the present invention, said copper alloy may include at least one of Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe, and said barrier metal may have at least one of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

[0084]

(Mode of Operation)

In the above-structured present invention, since silicon is diffused into a metal connection, the contact characteristics with a metal diffusion preventing film are

improved as compared with a case where silicon is not diffused. Also, since silicon is diffused, the migration during a manufacturing step is suppressed. Also, the anti-electromigration characteristics and anti-stress migration characteristics of a connection are improved. Further, since the metal connection into which silicon is diffused has a high anti-oxidation characteristic, the deterioration of a connection surface at an etching is suppressed.

[0085]

Also, in the present invention, since silicon is also diffused into a via plug, the contact characteristics with a metal diffusion preventing film are improved as compared with a case where silicon, the migration during a manufacturing step is further suppressed. Also, the anti-electromigration characteristics and anti-stress migration characteristics of a connection are further improved.

[0086]

Also, in the present invention, since the silicon concentration at the upper surface of the metal connection, the contact characteristics with its upper layer, i.e., the metal diffusion preventing film is further improved.

[0087]

Also, in the present invention, since a silicon concentration of said metal connection is not larger than 8 atoms %, the increase of the connection resistance as compared with that of a silicide layer is suppressed.

[0088]

Also, in the present invention, since an insulating film for insulating the same layer connections from each other includes at least one of a ladder-type hydrogen silozane and a porous ladder-type hydrogen silozane, the inter-connection capacitance can be decreased than that of an oxide film. Also,

when the film density is not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3, and the film refractive index is not smaller than 1.38 nm and not larger than 1.40 nm at a wavelength of 633 nm, the dielectric constant is further decreased.

[0089]

Also, in the present invention, since the metal diffusion preventing film includes at least one of SiCN, SiC, SiOC and an organic film, the contact characteristics between the metal connection into which silicon is diffused and the metal diffusion preventing film are good.

[0090]

Also, in the present invention, since the etching stopper film is used, overetching is avoided so that the shape of grooves formed at every etching process is definite.

[0091]

Also, in the present invention, since the insulating film for insulating different connection layers from each other includes at least one of SiO_2, SiOC and an organic film, the inter-connection capacitance can be decreased as compared with that of a nitride film.

[0092]

Also, in the present invention, since the etching stopper film uses at least one of a SiCN film, a SiC film, a SiOC film and an organic film, the inter-connection capacitance can be decreased as compared with that of a nitride film.

[0093]

Also, in the present invention, after the metal oxide layer on a surface of the metal connection removed, silicon is diffused into the metal connection without exposing to oxygen, so that a low-resistance metal connection including no oxygen can be obtained.

[0094]

Also, in the present invention, since a reducing gas is

used when removing a metal oxide layer, the metal oxide layer can be easily removed by the reducing operation to the metal oxide layer.

[0095]

Also, in the present invention, since a film including benzotriazole or benzotriazole derivative is used, the erosion preventing effect of metal is high.

[0096]

Further, in the present invention, since a metal connection is a connection including at least one of copper and copper alloy, the connection resistance is decreased and the anti-electromigration characteristic is improved.

[0097]

[Mode of Carrying-out the Invention]

(First embodiment)

A structure of the semiconductor device of a first embodiment of the present invention will be explained.

[0098]

Fig. 1 is a cross-sectional view illustrating a structure of the semiconductor device of the present invention.

[0099]

As illustrated in Fig. 1, a semiconductor device of this embodiment is constructed so that a silicon-including Cu connection 8 formed by diffusing silicon into a Cu connection is provided in a groove section formed on a SiO_2 insulating film 2 on an underlying insulating film 1 grown on a semiconductor substrate (not shown). Side surfaces and a bottom surface of the silicon-including copper (Cu) connection 8 is covered by a Ta/TaN film 5, and a SiCN film 9 serving as a Cu diffusion preventing film and a SiO_2 interlayer insulating film 10 for serving insulation between connection layers are sequentially formed on the upper surface of the silicon-including Cu connection 8. The semiconductor

device is constructed by transistors, diodes, resistors, capacitors and the like which are not shown, in addition to the silicon-including Cu connection 8 of Fig. 1.

[0100]

Next, a parallel-plate type plasma CVD apparatus used in forming films such as the silicon-including Cu connection 8 and the SiCN film 9 and the like at a manufacturing step of the semiconductor device of the first embodiment is explained. Note that films are formed on a semiconductor substrate.

[0101]

Fig. 2 is a cross-sectional view illustrating an embodiment of the parallel-plate type plasma CVD apparatus used in the first embodiment.

[0102]

The above-mentioned plasma CVD apparatus is constructed by a processing chamber 30 for carrying out a film growing processing on a semiconductor substrate 100, a heater 32 for maintaining the temperature of the semiconductor substrate 100 mounted in the processing chamber 30 at a definite value, a carrying means (not shown) for carrying the semiconductor substrate 100 into the processing chamber 30, a gas exhaust means 34 for maintaining the pressure in the processing chamber 30 at a definite value, a gas supplying section 36 for supplying a plurality of kinds of reaction gas to the processing chamber 30, a high frequency generator 42 for generating high frequency waves in the processing chamber 30, and a computer 38 for controlling the heater 32, the carrying means (not shown), the gas exhaust means 34, the gas supplying means 36 and the high frequency generator 42.

[0103]

The gas supplying section 36 is connected via a plurality of gas passage pipes 35 for supplying a plurality of kinds of reaction gas and a gas flow rate control means 37 to the

processing chamber 30.

[0104]

Provided in the processing chamber 30 are an upper plate electrode 40 and a lower plate electrode 41 opposing to each other, which are connected to the above-mentioned high frequency generator 42. Also, the lower plate electrode 41 incorporates the above-mentioned heater 32. The high frequency generator 42 generates a high frequency of a predetermined frequency and a high frequency power (RF power) between the upper plate electrode 40 and the lower plate electrode 41.

[0105]

When the SiCN film 9 is formed by the above-structured plasma CVD apparatus, the semiconductor substrate 100 mounted on the lower plate electrode 41 is caused to be a desired temperature by the heater 32, the kinds and flow rate of reaction gas are adjusted so as to make the chamber 30 to be in a desired gas atmosphere at a desired processing pressure, and then a desired high frequency RF power is applied to generate a reaction gas plasma in the processing chamber 30, to thereby form the SiCN film 9 on the semiconductor substrate 100.

[0106]

Note that, the above-mentioned plasma CVD apparatus can not only diffuse silicon for forming the silicon-including Cu connection 8 and form films such as the SiCN film 9, but also can remove films formed on the semiconductor substrate 100 by adjusting the processing conditions such as the gas atmosphere, the processing pressure, the processing temperature and the RF power. In order to be able to remove films formed on the semiconductor substrate 100, the above-mentioned plasma CVD apparatus is of a leaf-type which processes the semiconductor substrate 100 one by one.

[0107]

Next, a manufacturing method of the semiconductor device of the first embodiment is explained.

[0108]

Fig. 3 is a cross-sectional view illustrating the manufacturing step procedures of the semiconductor device of the first embodiment.

[0109]

A 500 nm thick SiO_2 film 2 is grown by a plasma CVD method on an underlying insulating film 1 on a semiconductor substrate (not shown) where semiconductor elements such as transistors and capacitors are formed. A photoresist 3 is coated on the grown SiO_2 insulating film 2, and a resist pattern 4 for a groove connection is formed by a photolithography technology on the grown SiO_2 insulating film 2 (Fig. 3(a)).

[0110]

Next, the SiO_2 insulating film 2 is etched by a dry etching technology using the groove connection resist pattern 4 to form a groove connection pattern in the SiO_2 insulating film 2. After that, the photoresist 3 is removed by an O_2 dry ashing for carrying out an oxygen plasma processing and a wet stripping for removing residual resist.

[0111]

Next, as illustrated in Fig. 3(b), a 30 nm thick Ta/TaN film serving as a barrier metal is grown on the exposed underlying insulating film 1 and the SiO_2 film 2, and a 100 nm thick Cu layer serving as a cathode underlying layer of electroplating method is grown by a sputtering method. After that, a Cu layer 6 is buried by an electroplating method in the groove connection pattern, and a heating process at 400℃ is carried out to crystallize the Cu layer.

[0112]

Next, as illustrated in Fig. 3(c), the Cu oxide layer 6 and the Ta/TaN film 6 on the SiO_2 insulating film 2 are removed by a CMP method to form a Cu connection 7. After the processing by the CMP method, a cleaning processing is carried out, so that the Cu connection 7 is exposed to the air, and oxygen in the air reacts with Cu to form a Cu oxide layer on the exposed surface of the Cu connection 7. Therefore, a plasma processing at a processing temperature of 200 to 450℃, at an NH_3 gas flow rate of 50 to 1000 sccm, at a processing pressure of not larger than 20 Torr (not larger than 2666.4 Pa) and at an RF power of 50 to 500W is carried out for 5 seconds to remove the Cu oxide layer on the surface of the Cu connection by reduction using hydrogen.

[0113]

Next, in the plasma CVD apparatus, a heating process is performed upon the Cu connection 7 for 120 seconds at a SiH_4 gas flow rate of 10 to 500 sccm, at a N_2 gas flow rate of 100 to 5000 sccm and at a processing pressure of not larger than 20 Torr without exposing the exposed surface of the Cu connection 7 from which the Cu oxide layer is removed to the air, to form a silicon-including Cu connection 8. Here, when forming the silicon-including Cu connection 8, Si is deposited on the SiO_2 insulating film 2 depending upon the heating processing condition of SiH_4, so that the deposited Si may invite a short-circuit between the Cu connection 7. Therefore, after the silicon-including Cu connection 8 is formed, in the above-mentioned CVD apparatus, a plasma processing is carried out for 3 seconds at a NH_3 gas flow rate of 50 to 1000 sccm, at a N_2 gas flow rate of 100 to 5000 sccm, at a processing pressure of not larger than 20 Torr and at an RF power of 50 to 500W without exposing the silicon-including Cu connection to the air, to nitrize Si deposited on the surface of the silicon-including Cu connection 8 and the SiO_2 insulating film

2.

[0114]

Next, after the above-mentioned nitrizing processing, in the above-mentioned plasma CVD apparatus, a 50 nm thick SiCN film 9 serving as a Cu diffusion preventing film is grown on the silicon-including Cu connection 8 and the SiO_2 insulating film 2 whose surfaces are nitrized by a plasma CVD method using reaction gas of $SiH(CH_3)_3$, CN_3 and He without exposing the silicon-including Cu connection 8 to oxygen.

[0115]

After that, in the above-mentioned plasma CVD apparatus, a 500 nm thick SiO_2 interlayer insulating film 10 serving as an interlayer insulating film is grown on the SiCN film 9, to form an interlayer insulating film on the silicon-including Cu connection 8 (Fig. 3(d)).

[0116]

Note that a method for removing the Cu oxide layer is to reduce the Cu oxide layer using NH_3 as reaction gas; however, the Cu oxide layer can be reduced by using other reducing gas such as hydrogen, and also, the Cu oxide layer can be etched by using at least one of N_2, He and Ar as reaction gas. In this case, the high frequency of the high frequency waves is not limited to the above-mentioned condition, and can be not smaller than 100 kHz and not larger than 13.56 MHz to remove the Cu oxide layer.

[0117]

Also, the above-mentioned silicon-including Cu connection 8 is formed by using SiH_4 as source gas; however, inorganic silane gas such as Si_2H_6 or SiH_2Cl_2 can be used in a gas atmosphere excluding O_2 at a processing temperature of not smaller than 200℃ and not larger than 450℃ and at a processing pressure of not larger than 20 Torr.

[0118]

Also, in this embodiment, since silicon is diffused into the Cu connection 7, the contact characteristics with the upper Cu diffusion preventing film are improved. Note that, in order to further improve the contact characteristics with the upper Cu diffusion preventing film, it is preferable that the silicon concentration of the silicon-including Cu connection 8 is maximum at its upper surface. Also, in order to suppress the connection resistance, it is preferable that the silicon concentration of the silicon-including Cu connection 8 is not larger than 8 atoms %.

[0119]

Here, the difference between Cu silicide and a silicon-including Cu connection is explained.

[0120]

Fig. 4 is a graph illustrating a phase diagram between silicon and Cu. From the phase diagram of Cu and Si as illustrated in Fig. 4, when the amount of included Si satisfies that the ratio of Cu and Si is not larger than 92:8, no Cu silicide is formed but a silicon-including Cu layer is formed. A connection by this silicon-including Cu layer is the silicon-including Cu connection.

[0121]

Also, after the formation of the silicon-including Cu connection 8, Si deposited on the silicon-including Cu connection 8 and the SiO_2 insulating film 2 is nitrized; however, Si etching by plasma processing using He gas or Ar gas can be carried out to etch the surface, to remove the deposited Si. If no Si is deposited, the above-mentioned nitrizing processing and the Si etching processing can be omitted.

[0122]

Also, although the SiCN film 9 is used as a Cu diffusion preventing film, a SiC film or an organic film can be used.

For example, the organic film is a Teflon organic polymer film and an amorphous carbon film which can be formed by a plasma CVD method.

[0123]

Also, since the silicon-including Cu connection 8 has an oxidation preventing effect, an insulating film including O such as a SiOC film can be used instead of the SiC film and the SiCN film.

[0124]

Also, in this embodiment, the removal of the Cu oxide layer, the formation of the silicon-including Cu connection, the formation of the Cu diffusion preventing film are carried out within the above-mentioned plasma CVD apparatus so as not to expose the surface of the Cu connection 7 to oxygen; however, these processings can be carried out in the same processing chamber within the plasma CVD apparatus or in a plurality of processing chambers provided in the apparatus which are connected by substrate transport passages where a vacuum is drawn. Further, the above-processings can be carried out in a CVD apparatus, an etching apparatus and a heating apparatus corresponding thereto where a vacuum is drawn. Even in separate apparatuses corresponding to the processings, since the substrate transport passages therebetween are vacuum-drawn, the Cu connection 7 and the silicon-including Cu connection 8 are never exposed to oxygen.

[0125]

In this embodiment, since the Cu connection 7 and the silicon-including Cu connection 8 are never exposed to oxygen from the removal of the Cu oxide layer to the formation of the Cu diffusion preventing film, an oxide layer is never formed on the Cu connection 7 and the silicon-including Cu connection 8. As a result, the silicon-including Cu connection 8 has better contact characteristics with the Cu diffusion

preventing film, so that migration of Cu particles within the silicon-including Cu connection 8 can be avoided, thus improving the anti-electromigration characteristics. Also, disconnection of the silicon-including Cu connection 8 by the stress of passivation films as upper layers can be avoided to improve the anti-stressmigration characteristics. Therefore, long-life connections can be formed.

[0126]

(Second embodiment)

In a second embodiment of the present invention, a step of forming an oxidation preventing layer to avoid oxidation of the Cu connection and a step of removing the oxidation preventing layer are added between the Cu connection forming step and the silicon-including Cu connection forming step of the first embodiment.

[0127]

Since the structure of a semiconductor device of this embodiment is similar to that of the first embodiment, its detailed description is omitted.

[0128]

A manufacturing method of the semiconductor device of the present invention is explained. Note that the description of similar steps to those of the first embodiment is omitted.

[0129]

As illustrated in Fig. 3(c), the Cu oxide layer 6 and the Ta/TaN film 6 on the SiO_2 insulating film 2 are removed by a CMP method to form a Cu connection 7. After the processing by the CMP method, a cleaning processing is carried out, so that abrasive grain adhered to the upper surface of the Cu connection 7 is removed, and a Cu oxide layer is formed by water used in the cleaning processing on the upper surface of the Cu connection 7. Subsequently, the exposed surface of the Cu oxide layer is immersed into a 1% diluted solution of BTA, so

that BTA reacts the Cu oxide film to form a BTA layer 11 serving as an oxidation preventing layer.

[0130]

Fig. 5 is a cross-sectional view illustrating a state of the BTA layer 11 formed on the Cu connection 7. Note that although an unreacted Cu oxide layer may remain under the BTA layer 11, the Cu oxide layer can be removed by oxalic acide or the like so that the Cu oxide layer can be suppressed to be not larger than several nm thick. In this embodiment, as illustrated, it is assumed that the BTA layer 11 is formed on the Cu connection 7.

[0131]

Next, in order to remove the BTA layer 11 on the Cu connection 7 by thermal decomposition, in the plasma CVD apparatus, a heat processing at a processing temperature of 200 to 450℃, at an N_2 gas flow rate of 10 to 5000 sccm and at a processing pressure of not larger than 20 Torr is carried out for 2 minutes. After the removal of the BTA layer 11, a silicon-including Cu connection 8 is formed without exposing the Cu connection 7 to oxygen in a similar way to the first embodiment.

[0132]

Hereinafter, processings are carried out in a similar way to the first embodiment to form a SiCN film 9 and a SiO_2 interlayer insulating film 10 (Fig. 3(d)).

[0133]

Although the heating processing for removing the BTA layer 11 on the surface of the Cu connection 7 is carried out in an N_2 gas atmosphere, a heating processing including at least one gas of NH_3, H_2, He, Ar and SiH_4 as reaction gas can be carried out in an atmosphere without O_2 gas. Also, if the reaction gas includes at least one of the above-mentioned NH_3, H_2 and SiH_4, even when a Cu oxide layer remains under the BTA layer 11, this

Cu oxide layer is easily removed by the reducing operation of hydrogen included in the reaction gas. Further, a heating processing can be carried out in a vacuum atmosphere without flowing any gas. In this heat processing, the BTA layer 11 can be removed at a temperature of not smaller than 200℃ and not larger than 450℃ and at a pressure of not larger than 20 Torr.

[0134]

Also, in this embodiment, although the BTA layer 11 is removed by a heating processing, the BTA layer 11 can be removed by a plasma processing in a gas atmosphere including at least one gas of N_2, NH_3, He and Ar as reaction gas. Also, in a similar way to the above-mentioned heating process, if a reducing gas is used, the Cu oxide layer is easily removed. In this plasma processing, the BTA layer 11 can be removed at a temperature of not smaller than 200℃ and not larger than 450℃, at a pressure of not larger than 20 Torr, at a frequency of 13.56 MHz of the high frequency waves and at an RF power of not smaller than 50W and not larger than 500W.

[0135]

Also, in a similar way to the first embodiment, it is preferable that the silicon concentration of the silicon-including Cu connection 8 ca be maximum at its upper surface, and, it is preferable that the silicon concentration of the silicon-including Cu connection 8 is not larger than 8 atoms %.

[0136]

In this embodiment, after the formation of the oxide preventing layer on the exposed surface of the Cu oxide layer on the Cu connection 7, a processing is carried out from the removal of the Cu oxide layer and the oxide preventing layer to the formation of the Cu diffusion preventing film, so that the Cu connection 7 and the silicon-including Cu connection 8 are never exposed to oxygen, and, thus, an oxide layer is

never formed on the Cu connection 7 and the silicon-including Cu connection 8. As a result, the silicon-including Cu connection 8 has better contact characteristics with the Cu diffusion preventing film, and, in a similar way to the first embodiment, the anti-electromigration characteristics and the anti-stressmigration characteristics are improved, thus forming long-life connections.

[0137]

(Third Embodiment)

A third embodiment of the present invention is characterized by applying a silicon-including copper connection to a double-connection of a dual damascene-structure by a VF method and applying a low dielectric constant interlayer insulating film to its inter-connection insulating film.

[0138]

The structure of the third embodiment will be explained.

[0139]

Fig. 6 is a cross-sectional view illustrating the structure of the semiconductor device of this embodiment.

[0140]

As illustrated in Fig. 6, the semiconductor device of this embodiment is constructed by connecting a first silicon-including copper connection 210 to a second silicon-including copper connection 223 via a via plug.

[0141]

The first silicon-including copper connection 210 is provided at a groove section formed in a stacked film. This groove section is formed in a stacked film formed by an underlying insulating film 201 grown on a semiconductor substrate (not shown), a SiC film 202, a ladder oxide film 203 made of ladder-type hydrogen siloxane, and a SiO_2 film 204. The side surface and bottom surface of the first

silicon-including copper connection 210 is covered by a Ta/TaN film 208. Hereinafter, note that the ladder oxide is referred to as L-Ox (NEC Corporation' s trademark).

[0142]

The via plug is provided at a hole section formed in a stacked film formed by a SiCN film 211 and a SiO_2 film 212 on the SiO_2 film 204. The side surface and bottom surface of the hole section is covered by a Ta/TaN film 220, and a silicon-including copper is buried therein.

[0143]

The second silicon-including copper connection 223 is provided at a groove section formed in a stacked film. This groove section is formed in a stacked film formed by the SiO_2 film 212, a SiC film 213, and a SiO_2 film 217. The side surface and bottom surface of the second silicon-including copper connection 223 is covered by a Ta/TaN film 220, and a SiCN film 222 is formed on the upper surface of the second silicon-including copper connection 223.

[0144]

Note that the semiconductor device is constructed by transistors, diodes, resistor, capacitor and the like which are not shown, in addition to the first silicon-including copper connection 210, the via plug and the second silicon-including copper connection 223.

[0145]

Next, a manufacturing method of the semiconductor device of this embodiment is explained.

[0146]

Figs. 7 to 10 are cross-sectional views illustrating manufacturing steps of the semiconductor device of the third embodiment. Note that the detailed description of similar steps to those of the first and second embodiments is omitted.

[0147]

In the manufacturing method of the semiconductor device of this embodiment, a 50 nm thick SiCN film 202 serving as an etching stopper for forming a groove section of a first groove connection is grown by a plasma CVD method on an underlying insulating film 201 grown on a substrate having semiconductor elements. Next, a 300 nm thick L-Ox film 203, which is a low dielectric interlayer insulating film of a first copper groove connection, is grown by a coating method, and is calcined for 30 minutes at a temperature of 400℃ in a N_2 atmosphere. Next, a 100 nm thick SiO_2 film 204 is grown by a plasma CVD method. Next, a resist pattern 206 for a first groove connection (Fig. 7(a)).

[0148]

Further, the SiO_2 film 204 and the L-Ox film 203 are etched by a dry etching technology from the resist pattern for a first groove connection to form a first groove connection pattern 207. After that, the photoresist 205 and the reflection preventing film 225 are removed by an O_2 dry ashing (Fig. 7(b)).

[0149]

Next, the SiCN film 202 serving as an etching stopper film is etched back by a dry etching, to perforate a conductive surface with the underlying semiconductor elements, and then, a wet stripping is carried out to remove etching residues, to form a first groove connection pattern 207. Next, a 30 nm thick Ta/TaN film 208 serving as a barrier metal is grown by a sputtering method, and then, a 100 nm thick Cu film 209 is grown by a sputtering method on the Ta/TaN film 208. After that, a 700 nm thick Cu film 209 is grown by an electroplating method and is buried in the first groove connection pattern 207. Then, a heating processing for crystalling is carried out for 30 minutes at a temperature of 400℃ in a N_2 atmosphere (Fig. 7(c)).

[0150]

Next, the Cu film 209 and the Ta/TaN film 208 on the SiO_2 film 204 are removed by CMP, and a surface processing by BTA solution is carried out to form a copper connection whose surface is subject to an oxidation preventing processing by the BTA solution (Fig. 7(d)).

[0151]

Next, in order to remove the BTA layer on the first copper connection by thermal decomposition, in the plasma CVD apparatus, in a similar way to the second embodiment, a heat processing at a processing temperature of 200 to 450℃, at an N_2 gas flow rate of 10 to 5000 sccm and at a processing pressure of not larger than 20 Torr is carried out for 2 minutes. Further, after the removal of the BTA layer, a heating processing is performed upon the first copper groove connection for 240 seconds under the condition that the SiH_4 gas flow rate is 10 to 500 sccm, the N_2 gas flow rate is 100 to 5000 sccm, the processing pressure is not larger than 20 Torr, without exposing the first copper connection to oxygen to form a first silicon-including Cu connection 210, and then, a 50 nm thick SiCN film 211 serving as a Cu diffusion preventing film is grown.

[0152]

Note, here is a measurement result of a silicon concentration of the first silicon-including copper connection 210. Fig. 11 is a graph showing a silicon concentration of the first silicon-including copper connection 210 in the depth direction. As illustrated in Fig. 11, the silicon concentration is maximum at the surface of the connection, and the deeper in bottom direction, the smaller the silicon concentration.

[0153]

Next, a 400 nm thick SiO_2 film 204 and a 50 nm thick SiCN

film 213 serving as an etching stopper are grown. Then, a 300 nm thick L-Ox film 216 serving as an interlayer insulating film of a second copper groove connection is coated thereon and calcined. Then, a 100 nm thick SiO_2 film 217 is grown. Next, a reflection preventing film 225 and a photoresist 214 are coated, and a resist pattern 215 for a via is formed in the photoresist by a photolithography technology (Fig. 8(e)).

[0154]

Next, the interlayer insulating film and the insulating film between different layers are etched by a dry etching technology from the resist pattern 215 for a via, and this etching is stopped above the SiCN film 211 on the first silicon-including copper connection 210 (Fig. 8(f)). In this case, there are vias where the etching is stopped above the SiCN film 211, and there are vias where the etching is not stopped at the SiCN film 211 to expose the first silicon-including copper connection 210 at the bottom of the vias.

[0155]

After that, the reflection preventing film 225, the photoresist 214 and resist residues are removed by an O_2 dry ashing and a wet stripping. In this case, at the bottom of the vias where the SiCN film 211 is fallen, the first silicon-including copper connection 210 is oxidized or eroded; however, in case of the first silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that a stable SiO_2 film 224 is formed in self-alignment to prevent oxidation and erosion of copper.

[0156]

Next, a reflection preventing film 225 and a photoresist 218 are coated, and a resist pattern 219 for a second groove connection is formed in the photoresist by a photolithography

technology (Fig. 9(g)).

[0157]

Subsequently, the SiO_2 film 217, the L-Ox film 216 and the reflection preventing film 225 are etched by a dry etching technology to reach the SiCN film 213 as an etching stopper from the resist pattern 219 for a second groove connection. After that, an O_2 dry ashing is carried out to remove the photoresist 218 for a second groove connection and the reflection preventing film 225, and an etching-back is carried out to remove the SiCN film 211 at the bottom of the vias. Next, a wet stripping is carried out to remove etching residues (Fig. 9(h)). In this case, at the bottom of the vias where the SiCN film 211 is fallen at the via etching step, the first silicon-including copper connection 210 is further oxidized or eroded; however, in case of the first silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that stable SiO_2 is formed in self-alignment to prevent oxidation and erosion of copper.

[0158]

After that, the self-aligned SiO_2 at the bottom of the vias is removed by an RF etching processing before the sputtering of a barrier, and then, a 30 nm thick Ta/TaN film 220 is grown by a sputtering method, and then, a 100 nm thick Cu film 221 for seed is grown by a sputtering method on the Ta/TaN film 220. After that, a 700 nm thick Cu film 221 is grown by an electroplating method (Fig. 9(i)). Next, as illustrated in Fig. 10(j), a second copper groove connection and a via plug are formed by a CMP method.

[0159]

Next, in a similar way to the first copper groove connection, the BTA layer is removed and SiH_4 is irradiated to form a second silicon-including copper connection 223. Then,

a 50 nm thick SiCN film 222 as a Cu diffusion preventing film is grown (Fig. 10(k)). In this case, as explained above, the silicon concentration is maximum at the surface of the connection, and the deeper in bottom direction, the smaller the silicon concentration.

[0160]

As explained above, in the first silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that stable SiO_2 is formed in self-alignment to prevent oxidation and erosion of copper at the etching step. Further, as compared with a case where Cu silicide is formed, since silicon is diffused into the film, even if the surface of the connection is etched, the Cu oxidation preventing effect is high.

[0161]

Next, the evaluation result of the via chain manufacturing yield of semiconductor devices by this embodiment is explained.

[0162]

Fig. 12 is a graph illustrating the evaluation result of the via chain manufacturing yield by a double connection.

[0163]

The graph of Fig. 12 shows that an excellent manufacturing yield was obtained as compared with a pure copper (pure Cu) connection, in a similar way to a copper connection where Cu silicide is formed (hereinafter, referred to as a silicide copper connection). Note that the silicide copper connection is disclosed in United States Patent 6211084, for example.

[0164]

Next, the evaluation result of the anti-electromigration characteristics and the anti-stress migration characteristics is explained.

[0165]

Fig. 13 is a graph showing a result of evaluation of the anti-electromigration characteristics and the anti-stress migration characteristics.

[0166]

The graph of Fig. 13 shows that the anti-electromigration characteristics and the anti-stress migration characteristics of a silicon-including copper connection is higher by one-digit as compared with those of a pure copper connection and a silicide copper connection.

[0167]

As illustrated in the above-mentioned evaluation result, the silicon-including copper connection formed by this embodiment improves an effect of suppressing motion of metal particules of a metal connection by diffusing silicon into the entire connection to form the silicon-including copper connection, as compared with a case where a silicide layer is formed at an uppermost surface.

[0168]

Here, the physical properties of the above-mentioned L-Ox is explained.

[0169]

Various low dielectric constant materials can be used as inter-connection insulating films for insulating connections at the same layer from each other and insulating films between different layers, i.e., between a lower connection and an upper connection; however, in view of preventing connection delay, it is preferable that the dielectric constant is not larger than 2.9 and the film density is lower. For example, it is preferable that the film density is not smaller than 1.50 g/cm^3 and not larger than 1.58 g/cm^3. Also, it is preferable that the refractive index at a wavelength of 633 nm is not smaller than 1.38 and not larger than 1.40. An example of such an insulating film material is the above-mentioned L-Ox.

[0170]

Fig. 14 is a table of the physical properties data of L-Ox.

[0171]

As illustrated in Fig. 14, the dielectric constant and refractive index of L-Ox are 2.9 and 1.39, respectively. Therefore, it is shown that L-Ox is preferable as inter-connection insulating films and interlayer insulating films. Note, the insulating film does not only use a single layer of L-Ox, but also uses a stacked film with a SiO_2 film or the like, because SiO_2 has a lower dielectric constant than a nitride film.

[0172]

Next, the structure of the ladder-type hydrogen siloxane is explained.

[0173]

Fig. 15 is a schematic diagram illustrating the structure of L-Ox having the structure of the ladder-type hydrogen siloxane. In Fig. 15, n is a positive number larger than or equal to 1.

[0174]

L-Ox is a polymer having a ladder-type molecular structure as illustrated in Fig. 15. The structure of L-Ox as illustrated in Fig. 15 is explained by an observation result of FT-IR carrying out identification and quantative analysis of material.

[0175]

Fig. 16 is a graph showing the observation result of FT-IR.

[0176]

The chart of Fig. 16 features a sharp spectrum of a Si-H bond appeared at a wave number of $830cm^{-1}$. This sharpness of the spectrum shows that L-Ox has a two-dimensional structure. Another peak of a Si-H bond seems to be at the proximity of a wave number of $870cm^{-1}$ on the higher wave number of this sharp

spectrum, but this spectrum is extremely small. This is also considered to show that an measured object material has a two-dimensional structure.

[0177]

Next, the calcination temperature condition dependency of the physical properties of L-Ox is explained.

[0178]

Fig. 17 is a graph illustrating the fluctuation of the physical properties as the calcination condition is changed. In Fig. 17, R.I. indicated by black-circled marks show the refractive index at a wavelength of 633 nm, and black-squared marks show the density. An experiment is carried out by calcination in an inactive gas atmosphere such as nitrogen at a temperature of not smaller than 200℃ and not larger than 450℃.

[0179]

The refractive index is a parameter directly affecting the dielectric constant, and is changed between 1.38 and 1.40. The refractive index showed a value larger than 1.40 at a temperature lower than 400℃.

[0180]

The density of L-Ox showed 1.50 to 1.58 g/cm^3 at a calcination temperature of not smaller than 200℃ and not larger than 400℃. The density showed a value of larger than 1.60 g/cm^3 at a temperature larger than 400℃. The density remarkably increases at a calcination temperature of larger than 400℃.

[0181]

Note that no measurement was carried out at a temperature of smaller than 200℃. At a temperature of smaller than 200℃, a spectrum of a bond which is expected to be a Si-OH (silanol) appearing at a wave number of about 3650cm^{-1} was observed in an FT-IR chart which is not shown, and Si-OH (silanol) is

considered to affect the physical properties.

[0182]

Thus, when growing an insulating film including L-Ox, it showed that L-Ox of excellent physical properties with a low dielectric constant was stably obtained.

[0183]

Next, the difference in structure between HSQ (hydrogen silsesquioxane, hereinafter, referred to as HSQ) having a known three dimensional hydrogen silsesquioxane structure and L-Ox is explained.

[0184]

Fig. 18 is a schematic diagram illustrating a molecular skeleton of HSQ (cited from "semiconductor technology outlook, 1998, p.431-435").

[0185]

In the materials of the above-mentioned two structures, there is a large difference in film stability in the manufacturing process, and L-Ox shows a more-remarkably excellent film stability. Because it is considered that the amount of decrease of Si-H in L-Ox is smaller than that in HSQ. Also, it is considered that the state of bonds of hydrogen atoms in the insulating film is different. That is, in HSQ, hydrogen atoms are bonded at peripheral portion of its cubic structure, while in L-Ox, hydrogen atoms are bonded at side faces of a ladder structure. Therefore, it is considered that the density around hydrogen atoms is lower in HSQ, and the hydrogen bonds of HSQ is more reactive than those of L-Ox.

[0186]

Next, the difference in film stability between L-Ox and HSQ is explained.

[0187]

Two kinds of connection structures were made by L-Ox and HSQ, and a silicon adding process by SiH_4 irradation was

carried out to confirm a large difference in anti-film properties. Hereinafter, this will be explained by experimental data.

[0188]

Note that SiH_4 irradation is carried out in a chamber of a plasma CVD apparatus under the conditions that the processing temperature is 200 to 450℃; the processing pressure is not larger than 20 Torr; the gas flow rate of SiH_4 = 10 to 500 sccm; and the gas flow rate of N_2 = 100 to 5000 sccm. In this experiment, HSQ and L-Ox using 300 nm thick blank wafers are baked at a hot plate of about 200℃ after coating, and then, are calcined in a diffusion furnace in a nitrogen atmosphere of 350℃ for 30 minutes. The thickness and refractive index were measured by a spectro elipsometer. The dielectric constant was calculated in accordance with the capacitance value measured in a mercury probe apparatus and the film thickness measured by the above-mentioned spectro elipsometer.

[0189]

Fig. 19(a) is a graph illustrating a film thickness contraction ratio amount to a SiH_4 irradation time; (b) is a graph illustrating a refractive index ratio amount to a SiH_4 irradation time; and (c) is a graph illustrating a dielectric constant change amount to a SiH_4 irradation time.

[0190]

As illustrated in Fig. 19(a), regarding the film thick contraction ratio, the thickness of L-Ox is hardly changed at 99% of an initial value from 0s to 120s. On the other hand, the thickness of HSQ is decreased as the SiH_4 irradation time is increased, so that it is decreased to about 80% of an initial value at an irradation time of 120s.

[0191]

As illustrated in Fig. 19(b), regarding the refractive

index, at a measurement by a wavelength of 633 nm, the refractive index of HSQ is changed from an initial value 1.39 to 1.42 at an irradation time of 120s. On the other hand, the refractive index of L-Ox is unchanged at an initial value 1.39 at an irradation time from 0s to 120s.

[0192]

As illustrated in Fig. 19(c), regarding the dielectric constant change, the dielectric constant of HSQ is increased from an initial value 2.9 to 3.4 at an irradation time of 120s. On the other hand, the dielectric constant of L-Ox is unchanged at an initial value 2.9 at an irradation time of 120s.

[0193]

From the above-mentioned results, L-Ox has excellent resistance to SiH_4 irradation in any of the film thickness, the refractive index and the dielectric constant. This difference in resistance to SiH_4 irradation is considered to be a difference in reaction of hydrogen bonds.

[0194]

In view of the foregoing, when carrying out a SiH_4 irradation processing, L-Ox as an interlayer is preferable as compared with HSQ. Also, it was confirmed that the same resistance for SiH_4 irradation processing as in L-Ox is applied to a porons L-Ox with a dielectric constant of 2.5.

[0195]

Further, regarding the resistance of L-Ox and HSQ for chemicals, since a comparison experiment was carried out, its result will be explained.

[0196]

Fig. 20(a) is a table illustrating film thickness after a definite amount is etched; and (b) is a schematic diagram illustrating measurement positions within a wafer. According to the experiment, after a wafer is immersed into an etching solution of fluoric ammonium and diluted HF for a definite time,

etching amounts at five positions ① to ⑤ as illustrated in Fig. 20 (b) were measured. In the table, unit of numerals is Angstrom ($\times 10^{-8}$ cm).

[0197]

When comparing the etching rates for fluoric ammonium and diluted HF, it was shown that the etching rate of L-Ox is larger than that of HSQ.

[0198]

Next, when a HSQ film and an L-Ox film are applied to inter-connection insulating films of an actual damascene connection structure, the result of SiH_4 irradation processing will be explained.

[0199]

In a location where the density of connections is high, since the polishing speed of the CMP processing is large, the mask SiO_2 film disappears or is made thin. As a result, when the connections are irradiated with SiH_4, the HSQ film and the L-Ox film below the plasma SiO_2 film are also irradiated with SiH_4. When a connection structure having a line/space = 0.2/0.2 μm is irradiated with SiH_4, the inter-connection capacitance of HSQ was decreased by only 2 to 3% as compared with a case of SiO_2, while, the inter-connection capacitance of L-Ox was sufficiently decreased to 8 to 12% as compared with a case of SiO_2. Further, it was confirmed that the inter-connection capacitance of porus L-Ox (k=2.5) is decreased by about 15 to 20% as compared with a case of SiO_2 film.

[0200]

As stated above, even in an actual connection structure, it was confirmed that L-Ox or porus L-Ox is preferable as compared with HSQ.

[0201]

Also, other materials such as MSQ (Methyl Silsesquioxane)

including carbon and an organic polymer having a principal structure of carbon were compared with an L-Ox film and a porus L-Ox film by using an actual damascene structure. In a damascene structure using a material including carbon such as an MSQ and an organic polymer, a thin copper oxide film was confirmed at an interface between a copper connection and a SiCN film as a cap film. Contrary to this, no copper film was confirmed between L-Ox films or porus L-Ox. This is because a small amount of oxygen is separated from L-Ox by heat within a chamber before the growth of a SiCN film, and this hydrogen is considered to reduce a copper oxide layer which has existed after CMP.

[0202]

Also, the film including carbon includes less hydrogen gas than L-Ox and more degassed hydrocarbon gas, so that the copper oxide film is expected to be not sufficiently reduced by the heat in the chamber before the growth of the SiCN film. Further, when a copper oxide layer is present in the film, it is expected that the anti-electromigration characteristics and the anti-stressmigration characteristics would deteriorate. That is, it is preferable that an L-Ox film or a porus L-Ox film is used as an interlayer film as compared with a carbon-including insulating film.

[0203]

(Fourth Embodiment)

A fourth embodiment is characterized by applying a silicon-including copper connection to a double-connection of a dual damascene-structure by an MF method and applying a low dielectric constant interlayer insulating film to its inter-connection insulating film. Note that, since the structure of the semiconductor device of this embodiment is similar to that of the third embodiment, its detailed description is omitted.

[0204]

A manufacturing method of the semiconductor device of this embodiment is explained.

[0205]

Figs. 21 to 23 are cross-sectional views illustrating manufacturing steps of the semiconductor device of the fourth embodiment. Note that the detailed description of similar steps to those of the first to third embodiments is omitted.

[0206]

In the manufacturing method of the semiconductor device of this embodiment, in a similar way to the third embodiment, a first silicon-including copper connection 210 is formed. In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in a bottom direction, the smaller the silicon concentration. Next, in a similar way to the third embodiment, a SiCN film 211 and a SiO_2 film 212 serving as an insulating film between different layer are sequentially formed. Further, a 50 nm thick SiCN film 213 serving as a second etching stopper is grown thereon (Fig. 21(a)).

[0207]

Next, in order to etch only the SiCN film 213 serving as the second etching stopper film to form a via pattern, a photoresist 214 is coated, and a resist pattern 215 for a via is formed by a photolithography technology in the photoresist 214 (Fig. 21(b)).

[0208]

Next, the SiCN film 213 is etched by a dry etching technology by using photoresist 214 as a mask. After that, the photoresist 214 and resist residues are removed by an O_2 dry ashing and a wet stripping. Next, a 300 nm thick L-Ox film 216 serving as an interlayer insulating film of a second copper groove connection is coated thereon and calcined. Then, a 100

nm thick SiO_2 film 217 is grown (Fig. 21(c)). Next, a photoresist 218 is coated, and a resist pattern 219 for a second groove connection is formed in the photoresist 218 by a photolithography technology (Fig. 22(d)).

[0209]

Next, the SiO_2 film 217 and the L-Ox film 216 serving as an interlayer insulating film for a second groove connection are etched by a dry etching technology using the photoresist 218 as a mask, and the SiO_2 film 212 serving as an insulating film between different layers is etched by the SiCN film 213 serving as a second etching stopper film where a via shaped pattern is formed, as an etching mask to reach the SiCN film 211 on the first silicon-including copper connection 210. After that, a wet stripping is carried out to remove etching residues (Fig. 22(e)).

[0210]

In this case, at the bottom of the vias where the SiCN film 211 is fallen at the etching step of the SiO_2 film 212, the connection is further oxidized or eroded; however, in case of the silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that a stable SiO_2 film is formed in self-alignment to prevent oxidation and erosion of copper.

[0211]

After that, the self-aligned SiO_2 film at the bottom of the vias is removed by an RF etching processing before the sputtering of a barrier, and then, a 30 nm thick Ta/TaN film 220 is grown by a sputtering method, and then, a 100 nm thick Cu film 221 for seed is grown by a sputtering method on the Ta/TaN film 220. After that, a 700 nm thick Cu film 220 is grown by an electroplating method (Fig. 22(f)). Next, as illustrated in Fig. 23(g), a second copper groove connection and a via plug are formed by a CMP method.

[0212]

Next, in a similar way to the first copper groove connection, the BTA layer is removed and SiH_4 is irradiated to form a second silicon-including copper connection 223. Then, a 50 nm thick SiCN film 222 as a Cu diffusion preventing film is grown (Fig. 23(h)). In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in a bottom direction, the smaller the silicon concentration.

[0213]

Note that, in the case of an MF method by this embodiment, a photolithography step is required to the SiCN film as an etching stopper film; however, since the surface of the SiCN film is hydrophilic so that the wettability of a reflection preventing film which is a coated film deteriorates, which easily invites unevenness and damages the SiCN film when the reflection preventing film is removed. Thus, a reflection preventing film can not be used. Also, in the photolithography step of the second groove connection, a large amount of a reflection preventing film is deposited at an etching step section of the etching stopper film, which is an obstacle in a dry etching step. Therefore, even in the photolithography step of the second groove connection, a reflection preventing film can not be used. Therefore, in the prior art copper connection, reflection from a lower layered Cu film can not be suppressed, which invites decrease of depth of focus (DOF) of a via. This is a problem. However, the silicon-including copper connection formed in this embodiment has a higher reflection preventing effect in photolithography steps than the prior art copper connection, so as to improve the photolithography step of an etching stopper film in an MF method, thus improving the manufacturing yield and the reliability.

[0214]

Here, a relationship between the silicon content and reflectivity is explained.

[0215]

Fig. 24 is a graph illustrating a relationship between silicon concentration and reflectivity. Note that, in reflection measurement, a Cu film including no silicon is used as a standard sample, while Cu films with various thicknesses into which the same amount of Cu is included are used as samples including silicon. The measurement is carried out by measuring reflectivity obtained by irradiating laser at a wavelength of 260 nm using a spectrophotometer.

[0216]

As illustrated in Fig. 24, the reflectivity of the surface of a copper including no silicon was 32%. The larger the silicon content, the smaller the reflectivity. The reflectivity was decreased to 2% at a silicon content of about 0.05%. Also, even when the silicon content was larger than that silicon content, the reflectivity was almost unchanged. From this result, when the silicon content is not smaller than 0.05%, it was shown that the effect is exhibited.

[0217]

Note that, in the third embodiment and this embodiment, in order to form a groove, after the interlayer insulating is etched by a dry etching, resist is removed by an O_2 dry ashing, and then, the SiCN film is etched back and etching residues are removed by a wet stripping; however, after the interlayer insulating film is etched by a dry etching, removal of resist and etching residues can be carried out by an O_2 dry ashing and a wet stripping, and then, the SiCN film can be etched back.

[0218]

(Fifth Embodiment)

A fifth embodiment is characterized by applying a silicon-including copper connection to a double-connection of

a dual damascene-structure by a TF method and applying a low dielectric constant interlayer insulating film to its inter-connection insulating film. Note that, since the structure of the semiconductor device of this embodiment is similar to that of the third embodiment, its detailed description is omitted.

[0219]

A manufacturing method of the semiconductor device of this embodiment is explained.

[0220]

Figs. 25 to 27 are cross-sectional views illustrating manufacturing steps of the semiconductor device of the fifth embodiment. Note that the detailed description of similar steps to those of the first to fourth embodiments is omitted.

[0221]

In the manufacturing method of the semiconductor device of this embodiment, in a similar way to the third embodiment, a first silicon-including copper connection 210 is formed. In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in bottom direction, the smaller the silicon concentration. Next, in a similar way to the third embodiment, a SiCN film 211 and a SiO_2 film 212 serving as an insulating film between different layer are sequentially formed. Further, a 50 nm thick SiCN film 213 serving as a second etching stopper is grown thereon.

[0222]

Next, a 300 nm thick L-Ox film 216 serving as an interlayer insulating film of a second copper groove connection is coated thereon and calcined. Then, a 100 nm thick SiO_2 film 217 is grown. Next, a reflection preventing film 225 and a photoresist 218 are coated, and a resist pattern 219 for a second groove connection is formed in the photoresist 218 by a photolithography technology (Fig. 25(a)).

[0222]

Next, the SiO_2 film 217 and the L-Ox film 216 serving as an interlayer insulating film for a second groove connection are etched by a dry etching technology using the photoresist 218 as a mask. After that, an O_2 dry ashing and a wet stripping are carried out to remove the photoresist 218, the reflection preventing film 225 and etching residues (Fig. 25(b)). Next, the SiCN film 213 as a second etching stopper is removed by an all-etching back (Fig. 25(c)).

[0224]

Next, a photoresist 214 is coated, and a resist pattern 215 for a via is formed by a photolithography technology in the photoresist 214 (Fig. 26(d)).

[0225]

Next, the SiO_2 film 212 serving as an insulating film between different layers is etched by a dry etching technology using the photoresist 214 as a mask to reach the SiCN film 211 on the first silicon-including copper connection 210. After that, the photoresist is removed by an O_2 dry ashing (Fig. 26(e)). Next, the SiCN film 211 on the first silicon-including copper connection 210 is etched back. After that, a wet stripping is carried out to remove etching residues (Fig. 26(f)).

[0226]

In this case, in a similar way to the fourth embodiment, at the bottom of the vias where the SiCN film 211 is fallen at the etching step of the SiO_2 film 212, the connection is further oxidized or eroded; however, in case of the silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that a stable SiO_2 film 224 is formed in self-alignment to prevent oxidation and erosion of copper.

[0227]

After that, the self-aligned SiO_2 film 224 at the bottom of the vias is removed by an RF etching processing before the sputtering of a barrier, and then, a 30 nm thick Ta/TaN film 220 is grown by a sputtering method, and then, a 100 nm thick Cu film 221 for seed is grown by a sputtering method on the Ta/TaN film 220. After that, a 700 nm thick Cu film 221 is grown by an electroplating method (Fig. 27(g)). Next, as illustrated in Fig. 27(h), a second copper groove connection and a via plug are formed by a CMP method.

[0228]

Next, in a similar way to the first copper groove connection, the BTA layer is removed and SiH_4 is irradiated to form a second silicon-including copper connection 223. Then, a 50 nm thick SiCN film 222 as a Cu diffusion preventing film is grown (Fig. 27(i)). In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in bottom direction, the smaller the silicon concentration.

[0229]

Note that, in the case of a TF method by this embodiment, a photolithography step is required for a via after the formation of the groove section of the second groove connection; however, if a reflection preventing film is used, the reflection preventing film is buried in the groove section of the second groove connection, the SiO_2 film, which is an lower insulating film between different layers, can not be etched. Thus, a reflection preventing film can not be used. Therefore, in the prior art copper connection, reflection from a lower layered Cu film can not be suppressed, which invites decrease of DOF of a via. This is a problem. However, the silicon-including copper connection formed in this embodiment has a higher reflection preventing effect in photolithography steps than the prior art copper connection, so as to improve the photolithography step of an etching stopper film in a TF

method, thus improving the manufacturing yield and the reliability.

[0230]

Also, in the above-mentioned third embodiment to this embodiment. an etching stopper film is used; however, if a processing time at an etching step of its upper film of the etching stopper film is controlled, the etching stopper film may be omitted. The omission of the etching stopper film can decrease the inter-connection capacitance.

[0231]

(Sixth Embodiment)

A sixth embodiment of the present invention is characterized by applying a silicon-including copper connection to a double-connection of a single damascene-structure and applying a low dielectric constant interlayer insulating film to its inter-connection insulating film.

[0232]

The structure of the sixth embodiment will be explained.

[0233]

Fig. 28 is a cross-sectional view illustrating the structure of the semiconductor device of this embodiment.

[0234]

As illustrated in Fig. 28, the semiconductor device of this embodiment is constructed by connecting a first silicon-including copper connection 210 to a second silicon-including copper connection 223 via a silicon-including copper plug.

[0235]

The first silicon-including copper connection 210 is provided at a groove section formed in a stacked film. This groove section is formed in a stacked film formed by an underlying insulating film 201 grown on a semiconductor

substrate (not shown), a SiC film 202, an L-Ox film 203, and a SiO_2 film 204. The side surface and bottom surface of the first silicon-including copper connection 210 is covered by a Ta/TaN film 208.

[0236]

The silicon-including copper plug 228 is provided at a hole section formed in a stacked film formed by a SiCN film 211 and a SiO_2 film 212 on the SiO_2 film 204. The side surface and bottom surface of the hole section is covered by a Ta/TaN film 226.

[0237]

The second silicon-including copper connection 223 is provided at a groove section formed in a stacked film. This groove section is formed in a stacked film formed by a SiC film 213 and a SiO_2 film 217. The side surface and bottom surface of the second silicon-including copper connection 223 is covered by a Ta/TaN film 220, and a SiCN film 222 is formed on the upper surface of the second silicon-including copper connection 223.

[0238]

Note that the semiconductor device is constructed by transistors, diodes, resistor, capacitor and the like which are not shown, in addition to the first silicon-including copper connection 210, the silicon-including copper plug 228 and the second silicon-including copper connection 223.

[0239]

Next, a manufacturing method of the semiconductor device of this embodiment is explained.

[0240]

Figs. 29 to 32 are cross-sectional views illustrating manufacturing steps of the semiconductor device of the sixth embodiment. Note that the detailed description of similar steps to those of the first to fifth embodiments is omitted.

[0241]

In the manufacturing method of the semiconductor device of this embodiment, in a similar way to the third embodiment, a first silicon-including copper connection 210 is formed. In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in a bottom direction, the smaller the silicon concentration.

[0243]

Next, in a similar way to the third embodiment, a SiCN film 211 and a SiO_2 film 212 serving as an insulating film between different layer are sequentially formed. Next, a reflection preventing film 225 and a photoresist 214 are coated on the grown SiO_2 film 212, and a resist pattern 215 for a via is formed by a photolithography technology (Fig. 29(b)).

[0244]

Next, the SiO_2 film 212 is etched by a dry etching technology by using the resist pattern for a via. After that, the photoresist 214 and the reflection preventing film 225 are removed by an O_2 dry ashing (Fig. 29(c)). Next, the SiCN film 211 at the via bottom is etched back. Next, etching residues are removed by a wet stripping (Fig. 29(d)).

[0245]

In this case, at the bottom of the vias where the SiCN film 211 is fallen at the etching step of the SiO_2 film 212, the first silicon-including copper connection 210 is oxidized or eroded; however, in case of the first silicon-including copper connection, silicon is first oxidized due to the difference of the electronegativity, so that a stable SiO_2 film 224 is formed in self-alignment to prevent oxidation and erosion of copper.

[0246]

After that, the self-aligned SiO_2 film 224 at the bottom of the vias is removed by an RF etching processing before the

sputtering of a barrier, and then, a 30 nm thick Ta/TaN film 226 is grown by a sputtering method, and then, a 100 nm thick Cu film 221 for seed is grown by a sputtering method on the Ta/TaN film 226. After that, a 700 nm thick Cu film 227 is grown by an electroplating method, and is buried in the via pattern, so that a heating processing at a temperature of 400℃ is carried out to crystallize.

[0247]

Next, the Cu film 227 and the Ta/TaN film 226 on the SiO_2 film 212 are removed by a CMP method, and further, a surface processing by BTA solution is carried out, so that the Cu surface is subject to a surface processing by BTA solution to form a copper via plug which is subject to an oxidation preventing process by a BTA layer (Fig. 30(g)).

[0248]

Next, in the same step for forming the first silicon-including copper connection 210 as in the third embodiment, a silicon-including copper plug 228 is formed, and then, a 50 nm thick SiCN film 213 as a second Cu diffusion preventing film is grown (Fig. 30(g)).

[0249]

Next, a 300 nm thick L-Ox film 216 serving as a second interlayer insulating film is coated thereon and calcined. Then, a 100 nm thick SiO_2 film 217 is grown. Next, a reflection preventing film 225 and a photoresist 218 are coated, and a resist pattern 219 for a second groove connection is formed in the photoresist by a photolithography technology (Fig. 31(h)).

[0250]

Next, the SiO_2 film 217 and the L-Ox film 216 serving as an interlayer insulating film for a second groove connection are etched by a dry etching technology using the photoresist 218 as a mask. Next, the photoresist 218 and the reflection

preventing film 225 are removed by an O_2 dry ashing. Next, an entire etching back is carried out to remove the SiCN film 213 of the second Cu diffusion preventing film. Next, etching residues are removed by wet stripping (Fig. 31(i)).

[0251]

In this case, in a similar way to a via etching step, at the bottom of the second groove connection where the SiCN film is fallen, the connection is further oxidized or eroded; however, in case of the silicon-including copper plug, silicon is first oxidized due to the difference of the electronegativity, so that a stable SiO_2 film is formed in self-alignment to prevent oxidation and erosion of copper.

[0252]

After that, the self-aligned SiO_2 film at the bottom of the vias is removed by an RF etching processing before the sputtering of a barrier, and then, a 30 nm thick Ta/TaN film 220 is grown by a sputtering method, and then, a 100 nm thick Cu film 221 for seed is grown by a sputtering method on the Ta/TaN film 220. Next, a 700 nm thick Cu film 221 is grown by an electroplating method (Fig. 31(j)). Next, a second copper groove connection is formed by a CMP method, and a surface processing by BTA solution is carried out (Fig. 32(k)).

[0253]

Next, in a similar way to the first silicon-including copper connection 210 and the silicon-including copper 228, the BTA layer is removed and SiH_4 is irradiated to form a second silicon-including copper connection 223. Then, a 50 nm thick SiCN film 222 as a Cu diffusion preventing film is grown (Fig. 32(l)). In this case, the silicon concentration is maximum at the surface of the connection, and the deeper in a bottom direction, the smaller the silicon concentration.

[0254]

As explained above, the connections formed in this

embodiment, since silicon is diffused into the entire connections to form silicon-including metal connections, the effect for suppressing the motion of metal particles in the metal connections can be enhanced as compared with a case where a silicide layer is formed at an uppermost surface.

[0255]

Also, in the silicon-including copper connection formed by this embodiment, since silicon is first oxidized due to the difference of the electronegativity, so that stable SiO_2 is formed in self-alignment to prevent oxidation and erosion of copper at the etching step, the manufacturing yield can be enhanced as compared with a pure copper connection.

[0256]

Further, in this embodiment, since one silicon-including copper connection having a high concentration of silicon at its upper surface is formed in the first groove connection, the second groove connection and the via plug by a single damascene structure, the silicon concentration within the via can be higher as compared with those formed by a dual damascene structure.

[0257]

Here, the evaluation result of the anti-electromigration characteristics and the anti-stressmigration characteristics is explained.

[0258]

Fig. 33 is a graph illustrating the evaluation result of the anti-electromigration characteristics and the anti-stressmigration characteristics.

[0259]

As illustrated in Fig. 33, the anti-electromigration characteristics and the anti-stress migration characteristics of the silicon-including copper connections by this embodiment are further improved as compared with those

manufactured by a dual damascene structure.

[0260]

Note that, in the fifth embodiment and this embodiment, in order to form a groove and a via, after the interlayer insulating is etched by a dry etching, resist is removed by an O_2 dry ashing, and then, the SiCN film is etched back and etching residues are removed by a wet stripping; however, after the interlayer insulating film is etched by a dry etching, removal of resist and etching residues can be carried out by an O_2 dry ashing and a wet stripping, and then, the SiCN film can be etched back.

[0261]

In the above-described third embodiment to this embodiment, an insulating film between different layers is used as a SiO_2 film; however, a stacked film formed by an L-Ox film and a SiO_2 film can be used in a similar way to an insulating film between groove connection layers. Also, a SiO_2 film is used as a mask insulating film of an L-Ox film, insulating films such as a SiC film, a SiCN film and a SiOC film can be used, if they have an excellent etching selectivity, and excellent anti-O_2 dry ashing and anti-wet stripping liquid characteristics. Further, L-Ox is used as an low dielectric constant interlayer insulating film; however, an insulating film such as a SiOF film, a SiOC film and an organic film having a lower specific dielectric constant than that of SiO_2 can be used.

[0262]

In the above-mentioned first to sixth embodiments, a copper connection is used; however, a connection including copper and other metals such as a metal connection including copper alloy including at least one of different kinds of elements: Al, Ag(silver), W(tungsten), Mg(magnesium), Be(beryllium), Zn(zinc), Pd(palladium), Cd(cadmium),

Au(gold), Hg(mercury), Pt(platinum), Zr(zirconium), Ti(titan), Sn(tin), Ni(nickel) and Fe(iron) can be used, and also, other metal connections can be applied. Even in this case, the anti-electromignation characteristics and the anti-stressmignation characteristics never deteriorate.

[0263]

In the above-mentioned first to sixth embodiments, a Ta/TaN film is used as a barrier metal; however, the barrier metal can include at least one of Ti, TiN, TiSiN, Ta, TaN and TaSiN. Even in this case, the anti-electromignation characteristics and the anti-stressmigantion characteristics never deteriorate.

[0264]

Also, in order to form an oxidation preventing film on a connection surface, BTA is used; however, BTA derivative having a higher solubility can be used.

[0265]

Also, the semiconductor device of the present invention is a semiconductor device having a copper connection; however, the semiconductor device may not need transistors, diodes, resistors, capacitors and the like.

[0266]

[Effect of the Invention]

The present invention has the above-described structures, and therefore, has the following effects.

[0267]

Since the manufacturing method of a semiconductor device of the present invention has good contact characteristics between a silicon-including metal connection and a metal diffusion preventing layer, metal particles of the metal connection are stabilized to improve the anti-electromigration characteristics. Also, the disconnection of the metal connection by a stress of a

passivation film or the like on its upper layer is avoided to improve the anti-stressmigration characteristics. Therefore, metal connection with a long life time can be formed.

[0268]

Also, in the present invention, since silicon is diffused into an entire connection to form a silicon-including metal connection, an effect for suppressing the motion of metal particles in the metal connection can be enhanced as compared with a case where a silicide layer is formed on an uppermost surface of a connection. Also, since the silicon content amount of the entire connection can be decreased as compared with case where a silicide layer is formed, the increase of a connection resistance can be suppressed.

[0269]

Also, the silicon-including copper connection of the present invention can avoid the oxidation and erosion of copper during an etching step. Further, since silicon is diffused into the interior of the film as compared with a case where a silicide layer is formed, even when the surface of a connection is etched, the copper oxidation preventing effect is high to suppress the deterioration of the connection by etching, thus improving the manufacturing yield.

[0270]

Also, since the silicon-including copper connection of the present invention has a high reflection preventing effect at a lithography step, the manufacturing yield and the reliability can be improved even at a lithography step where no reflection preventing film can be used.

[0271]

Further, even when the size of a connection is decreased by using a Cu connection as a metal connection, the increase of resistance of the connection is suppressed.

[BRIEF DESCRIPTION]

[Fig. 1]

A cross-sectional view illustrating the structure of a semiconductor device of a first embodiment.

[Fig. 2]

A cross-sectional view schematically illustrating an embodiment of the structure of a parallel-plate type plasma CVD apparatus used in the first embodiment.

[Fig. 3]

A cross-sectional views illustrating manufacturing steps of the semiconductor device of the first embodiment.

[Fig. 4]

A phase diagram of copper and silicon.

[Fig. 5]

A cross-sectional view illustrating a state where an oxidation preventing layer is formed on a Cu connection in a second embodiment of the present invention.

[Fig. 6]

A cross-sectional view illustrating the structure of a semiconductor device of a third embodiment.

[Fig. 7]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the third embodiment.

[Fig. 8]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the third embodiment.

[Fig. 9]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the third embodiment.

[Fig. 10]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the third embodiment.

[Fig. 11]

An experimental data diagram illustrating silicon

diffused into a copper connection by performing an SIMS analysis upon a silicon-including copper connection of the present invention.

[Fig. 12]

An experimental data diagram comparing a via chain manufacturing yield of a product formed by the third embodiment of the present invention with that of the priory art product.

[Fig. 13]

An experimental data diagram comparing a via EM of a product formed by the third embodiment of the present invention with that of the priory art product.

[Fig. 14]

A table illustrating physical properties data of L-Ox.

[Fig. 15]

A schematic view illustrating the structure of L-Ox.

[Fig. 16]

A graph illustrating the observation result of FI-IR.

[Fig. 17]

A graph illustrating the fluctuation of the physical properties as the calcinations condition is changed.

[Fig. 18]

A schematic diagram of the structure of HSQ.

[Fig. 19]

Experimental data diagrams of the thickness contraction rate fluctuation, the refractive index fluctuation and the specific dielectric constant fluctuation of HSQ and L-Ox to the SiH_4 irradation processing time of the present invention.

[Fig. 20]

A table illustrating the film thickness measurement result after etching of a definite amount and a schematic diagram illustrating measurement points.

[Fig. 21]

Cross-sectional views illustrating manufacturing steps of a semiconductor device of a fourth embodiment.

[Fig. 22]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the fourth embodiment.

[Fig. 23]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the fourth embodiment.

[Fig. 24]

An experimental data diagram review the relationship between the silicon concentration and the reflectivity in a silicon including copper connection of the present invention.

[Fig. 25]

Cross-sectional views illustrating manufacturing steps of a semiconductor device of a fifth embodiment.

[Fig. 26]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the fifth embodiment.

[Fig. 27]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the fifth embodiment.

[Fig. 28]

Cross-sectional views illustrating manufacturing steps of a semiconductor device of a sixth embodiment.

[Fig. 29]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the sixth embodiment.

[Fig. 30]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the sixth embodiment.

[Fig. 31]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the sixth embodiment.

[Fig. 32]

Cross-sectional views illustrating manufacturing steps of the semiconductor device of the sixth embodiment.

[Fig. 33]

An experimental data diagram comparing the via EM of products of a dual damascene structure with that of a single damascene structure in a silicon-including copper connection of the present invention.

[Fig. 34]

A cross-sectional view illustrating an embodiment of the structure of a prior art groove connection.

[Fig. 35]

Cross-sectional views illustrating manufacturing steps of a prior art VF method.

[Fig. 36]

Cross-sectional views illustrating manufacturing steps of the prior art VF method.

[Fig. 37]

Cross-sectional views illustrating manufacturing steps of the prior art VF method.

[Fig. 38]

An experimental data diagram illustrating a relationship between the via chain manufacturing yield and the rework number at a photolithography step of a second groove connection in products formed by the prior art VF method.

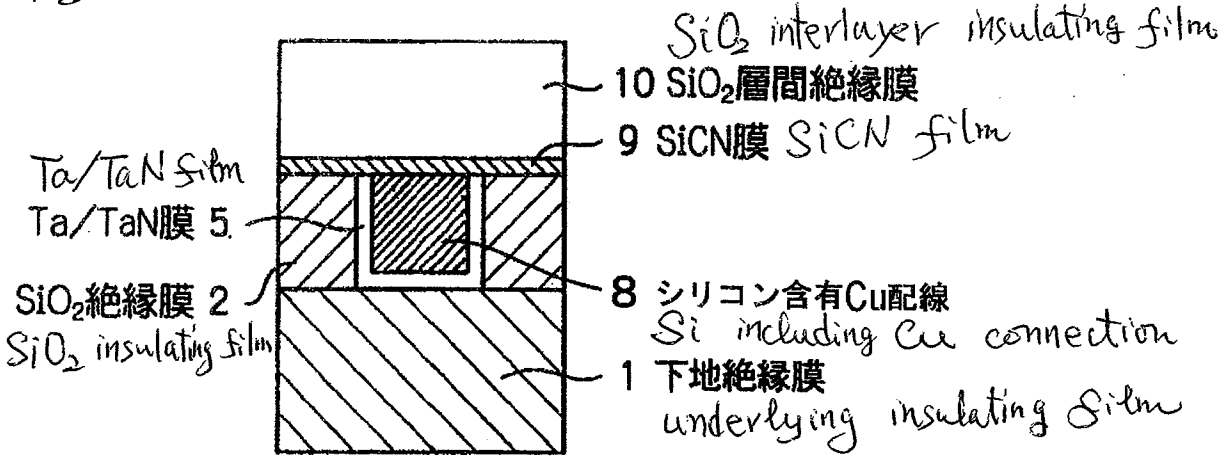
[Description of the Symbols]

1, 101, 201, 301	underlying insulating film
2, 102	SiO_2 insulating film
3, 205,214,218,314,318	photoresist
4	resist pattern for groove connection
5, 208, 220, 226, 320	Ta/TaN film
6	Cu film
7, 107	Cu connection

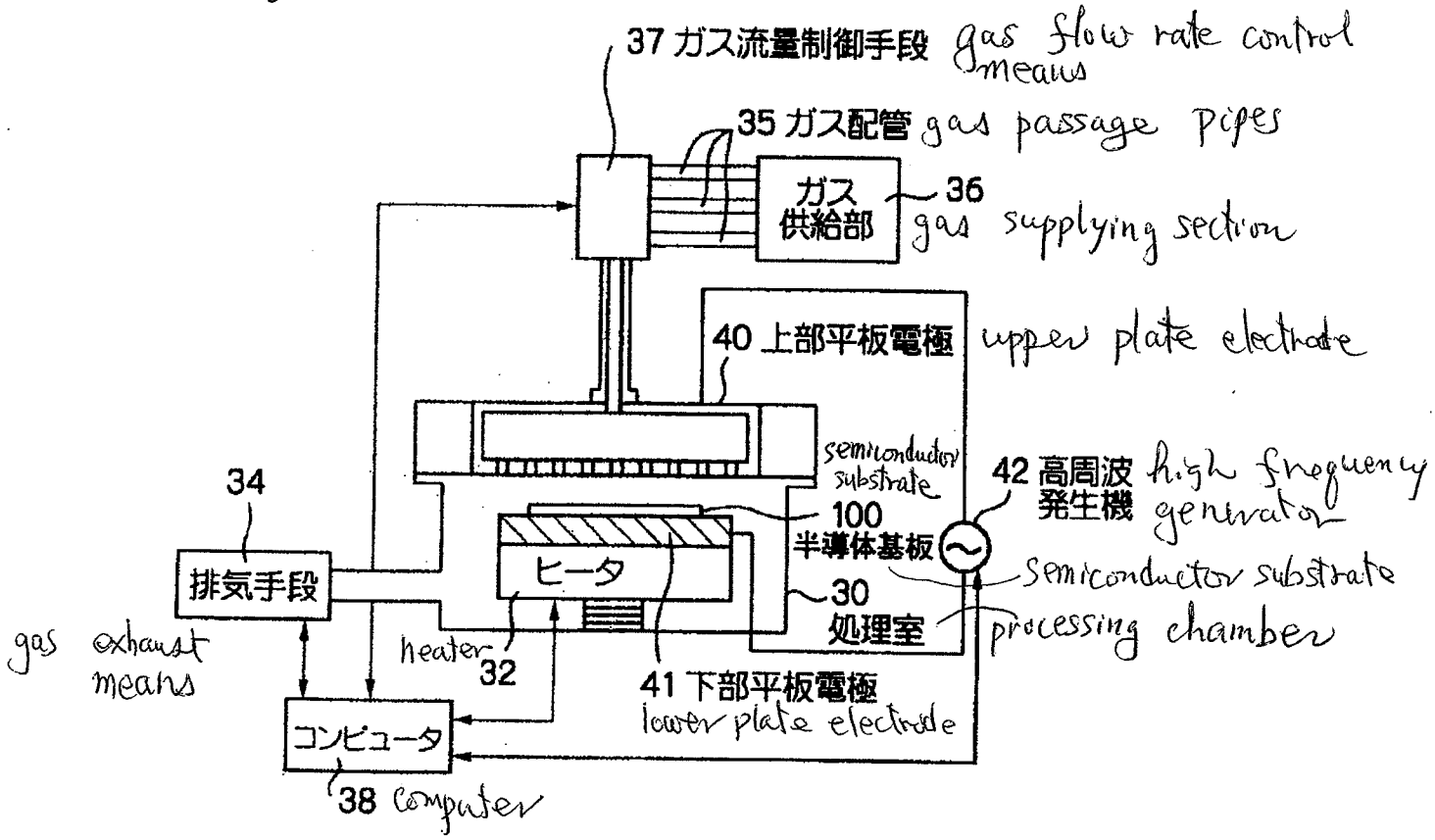
8 silicon-including Cu connection
9, 202,211,213,222,302,311,313,322 SiCN film
10, 110 SiO_2 interlayer insulating film
11 BTA layer
12, 112 SiN film
30 processing chamber
32 heater
34 gas exhausting means
35 gas pipe
36 gas supplying section
37 gas flow rate control means
38 computer
40 upper plate electrode
41 lower plate electrode
42 high frequency generator
100 semiconductor substrate
105 barrier metal
204,212,217,304,312,317 SiO_2 film
209,221,227,321 Cu film
203, 216 L-Ox
206 resist pattern for first groove connection
207 first groove connection pattern
215, 315 resist pattern for via
210 first silicon-including copper connection
219,319 resist pattern for second groove connection
223 second silicon-including copper connection
224 self-aligned SiO_2 film
225, 325 reflection preventing film
228 silicon-including copper plug
330 first copper connection
331 copper oxide layer
332 second copper connection

【書類名】 図面 Drawings
NAME OF DOCUMENT

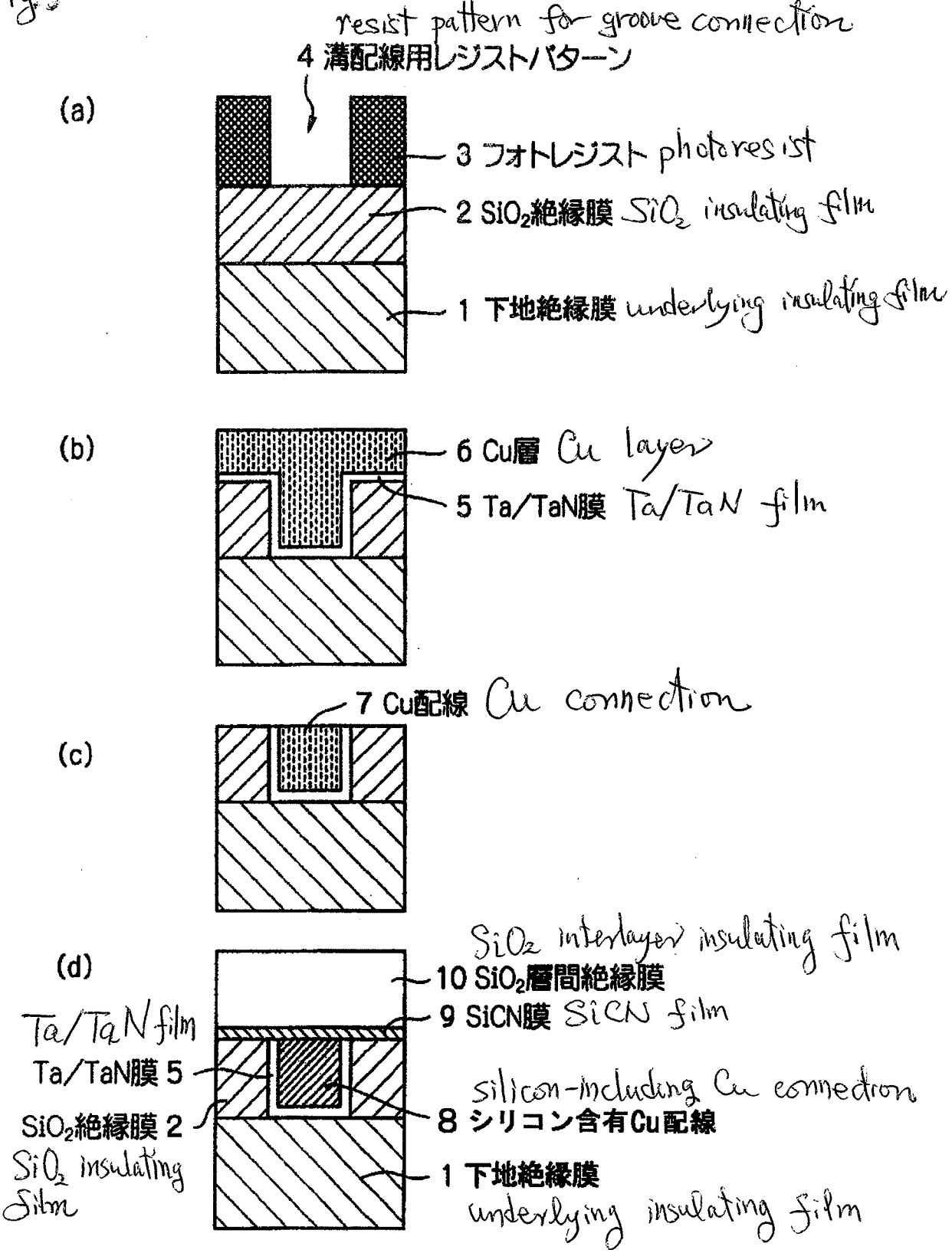
【図１】Fig. 1



【図２】Fig. 2



【図３】Fig. 3


resist pattern for groove connection
4 溝配線用レジストパターン
(a)
3 フォトレジスト photoresist
2 SiO2絶縁膜 SiO2 insulating film
1 下地絶縁膜 underlying insulating film
(b)
6 Cu層 Cu layer
5 Ta/TaN膜 Ta/TaN film
7 Cu配線 Cu connection
(c)
SiO2 interlayer insulating film
(d)
10 SiO2層間絶縁膜
9 SiCN膜 SiCN film
Ta/TaN film
Ta/TaN膜 5
silicon-including Cu connection
8 シリコン含有Cu配線
SiO2絶縁膜 2
SiO2 insulating film
1 下地絶縁膜
underlying insulating film

【図4】 Fig. 4

Crystal Structures. Lattice parameters of the α phase were reported by [6, 19, 13, 16, 27]; the parameter increases from $a = 3.615$ A at 0% Si to $a = 3.622$ A at 11.7 at. % Si [6, 16].

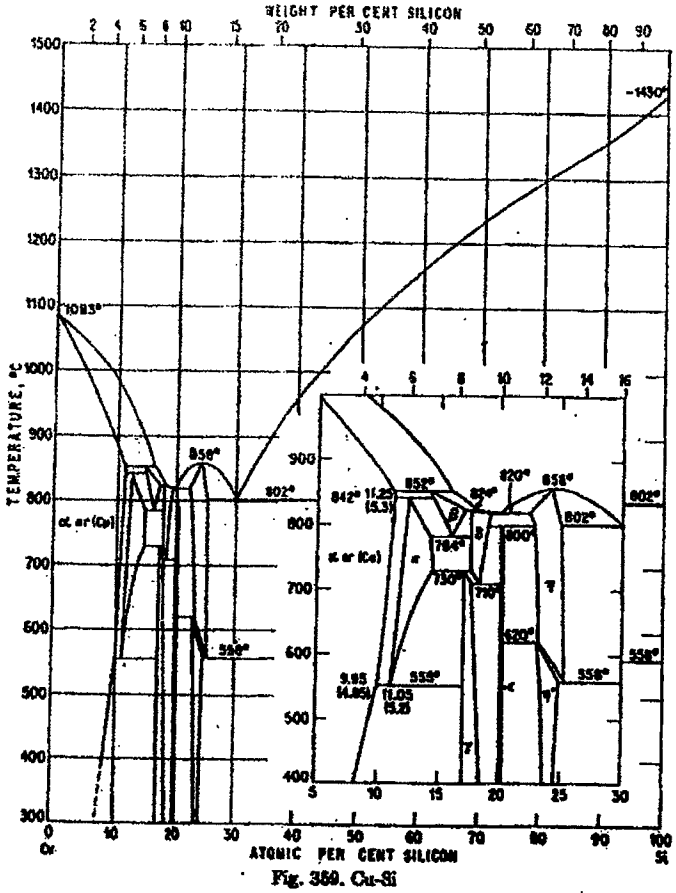


Fig. 359. Cu-Si

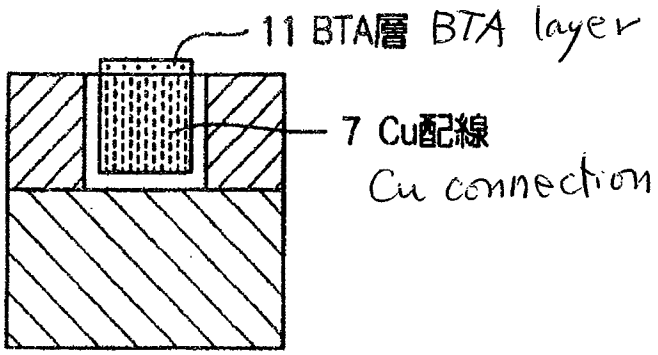
The α phase is h.c.p. (A3 type) [6, 8, 13, 16], with $a = 2.559$ A, $c = 4.185$ A, $c/a = 1.635$ at 11.8 at. % Si and $a = 2.562$ A, $c = 4.182$ A, $c/a = 1.632$ at 14.0 at. % Si [16].

The β phase, a 3:2 electron compound [28], is b.c.c. of the A2 type, $a = 2.854$ A at 14.9 at. % Si [13].

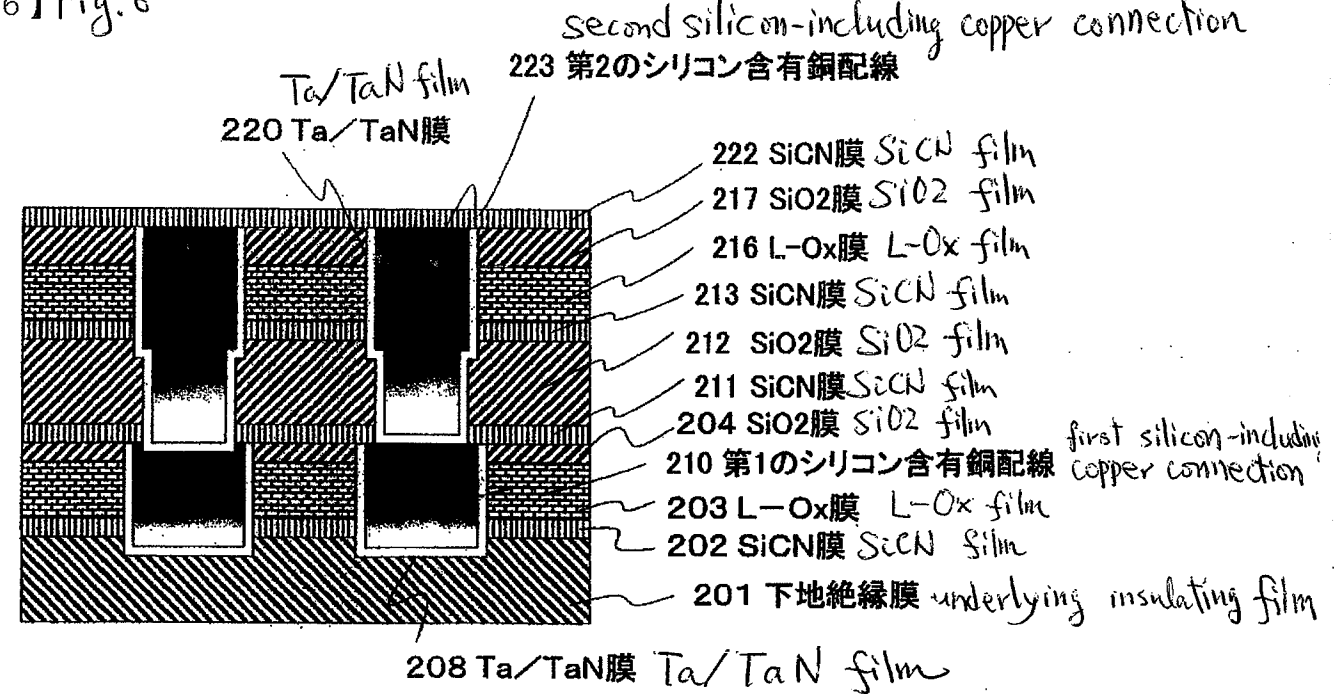
The γ phase is cubic of the β-Mn (A13) type [6, 8, 29, 14], $a = 6.222$ A [5, 29], $a = 6.193$ A [14].

Cu-Si相図 Cu-Si phase diagram

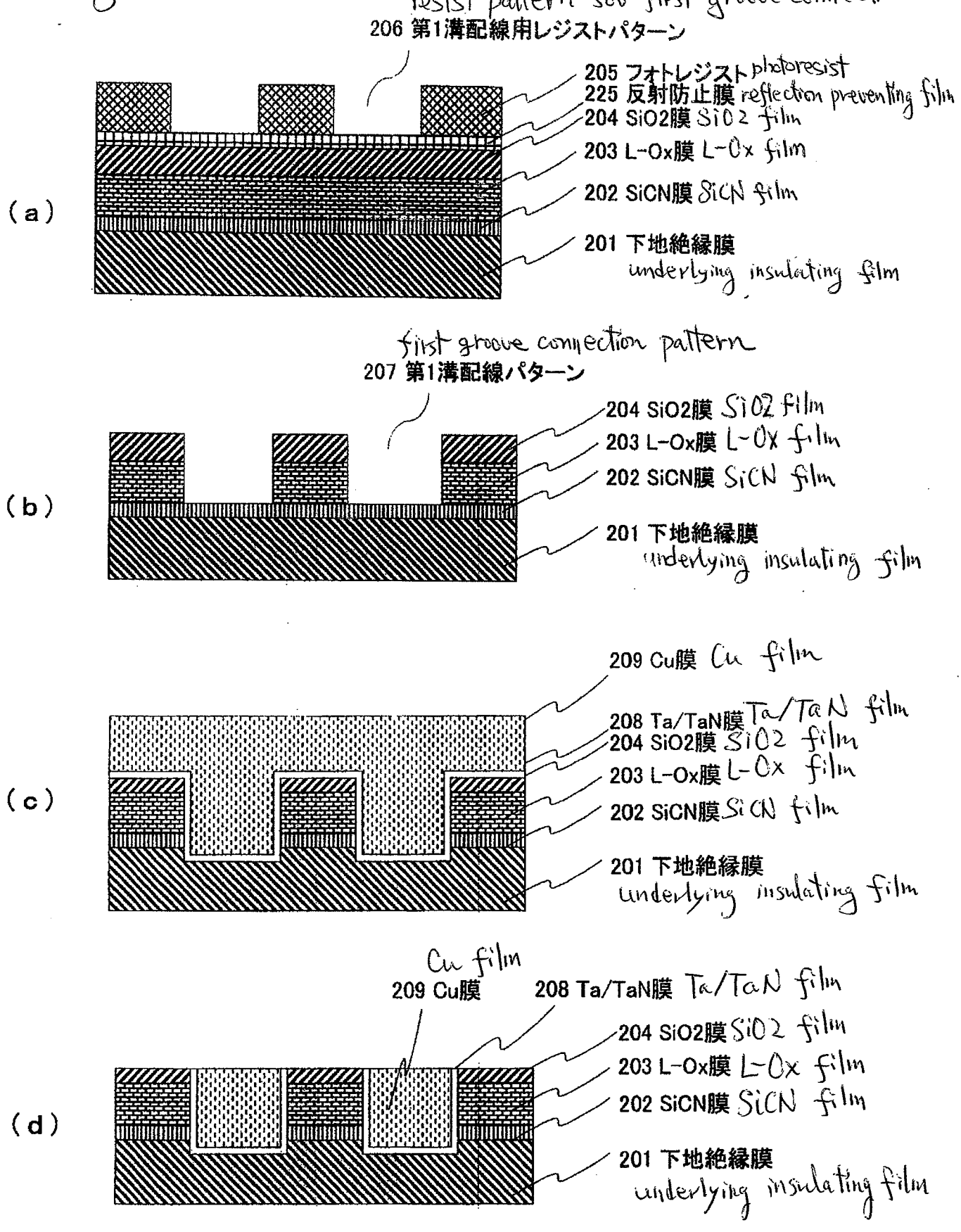
【図５】Fig.5



【図６】Fig.6

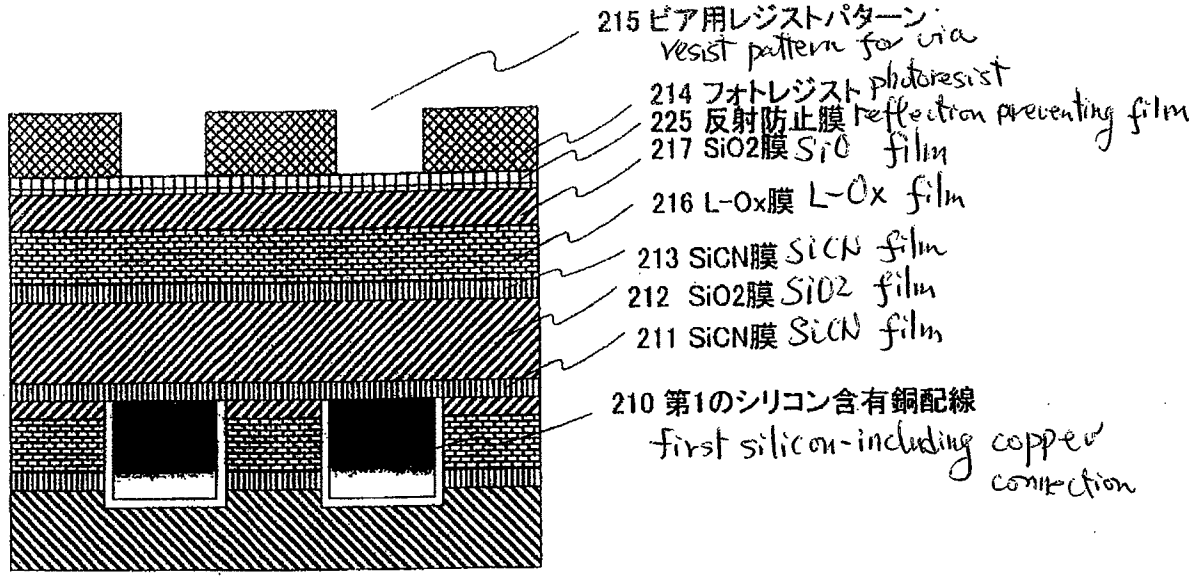


【図７】Fig. 7

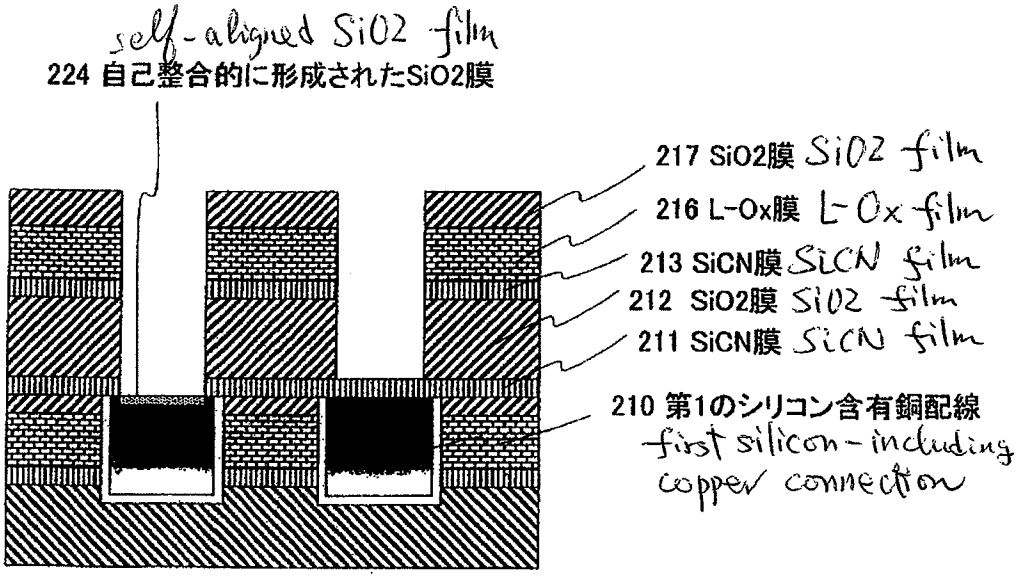

resist pattern for first groove connection
206 第1溝配線用レジストパターン
205 フォトレジスト photoresist
225 反射防止膜 reflection preventing film
204 SiO2膜 SiO2 film
203 L-Ox膜 L-Ox film
202 SiCN膜 SiCN film
201 下地絶縁膜
underlying insulating film
(a)
first groove connection pattern
207 第1溝配線パターン
204 SiO2膜 SiO2 film
203 L-Ox膜 L-Ox film
202 SiCN膜 SiCN film
201 下地絶縁膜
underlying insulating film
(b)
209 Cu膜 Cu film
208 Ta/TaN膜 Ta/TaN film
204 SiO2膜 SiO2 film
203 L-Ox膜 L-Ox film
202 SiCN膜 SiCN film
201 下地絶縁膜
underlying insulating film
(c)
Cu film
209 Cu膜
208 Ta/TaN膜 Ta/TaN film
204 SiO2膜 SiO2 film
203 L-Ox膜 L-Ox film
202 SiCN膜 SiCN film
201 下地絶縁膜
underlying insulating film
(d)

【図８】 Fig. 8

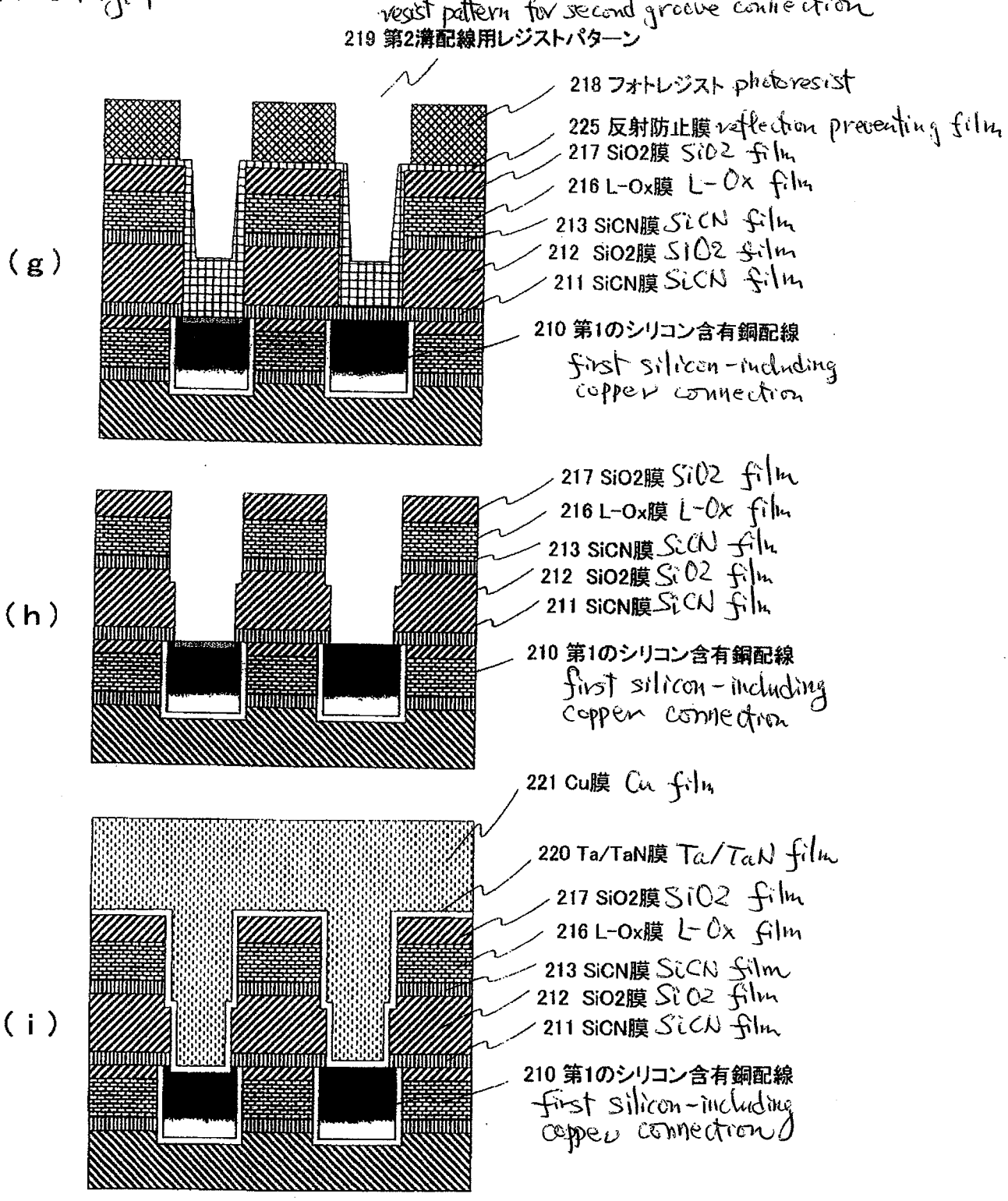
(e)


215 ビア用レジストパターン
resist pattern for via
214 フォトレジスト photoresist
225 反射防止膜 reflection preventing film
217 SiO2膜 SiO film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

(f)

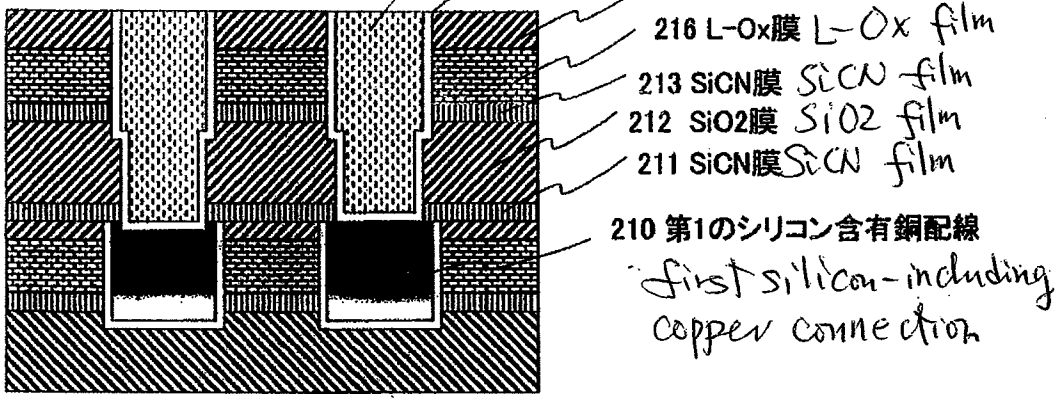

self-aligned SiO2 film
224 自己整合的に形成されたSiO2膜
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

【図９】 Fig. 9

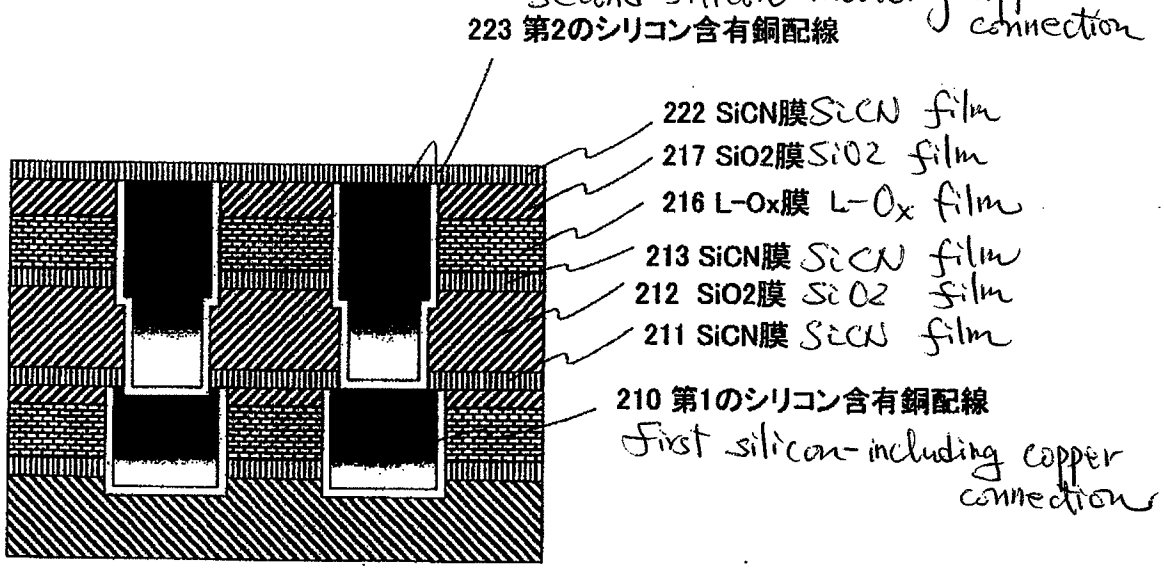

resist pattern for second groove connection
219 第2溝配線用レジストパターン
218 フォトレジスト photoresist
225 反射防止膜 reflection preventing film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(g)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(h)
221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(i)

【図１０】Fig. 10

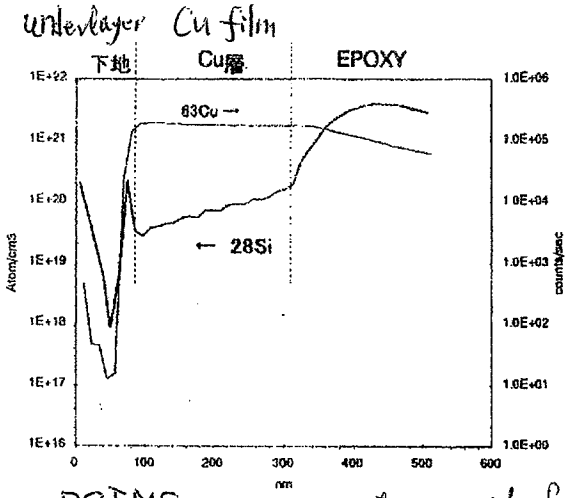
(j)


221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

(k)


second silicon-including copper connection
223 第2のシリコン含有銅配線
222 SiCN膜 SiCN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

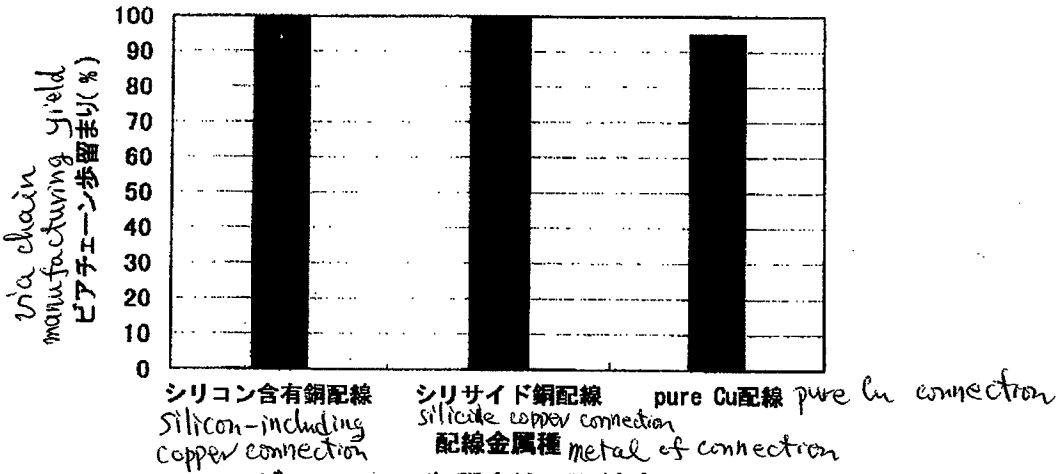
【図１１】Fig. 11



BSIMS measurement result of silicon-including copper connection

シリコン含有銅配線のBSIMS測定結果

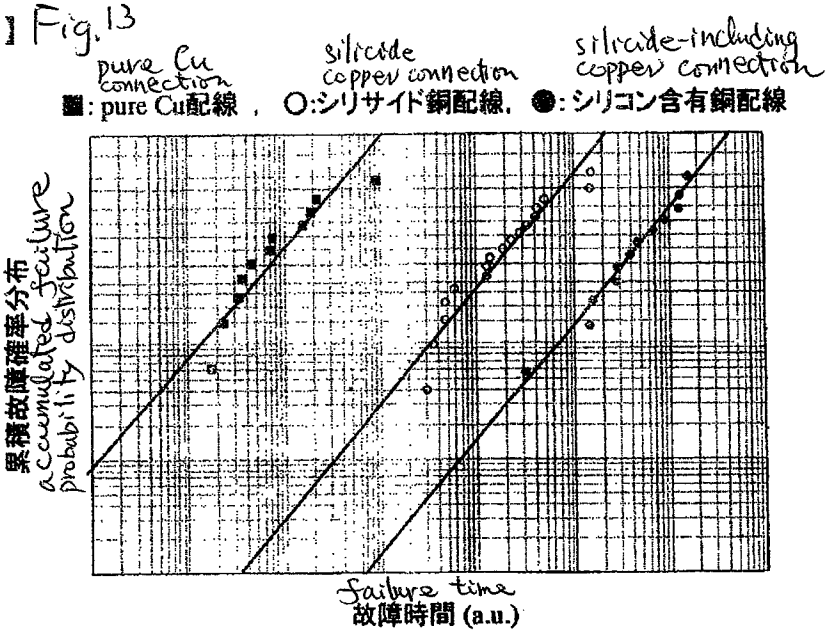
【図１２】Fig. 12



ビアチェーン歩留まりの配線金属種依存性

dependence of via chain manufacturing yield on metal of connection

【図１３】Fig.13



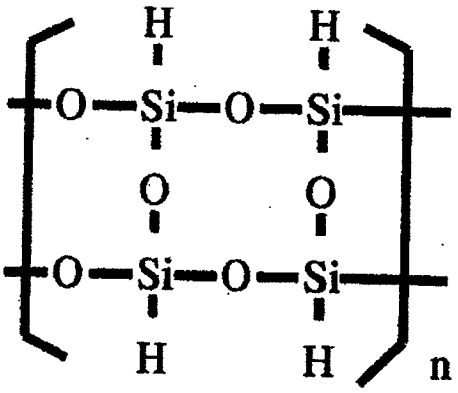
ビアEMの配線金属種依存性

dependence of via EM on metal of connection

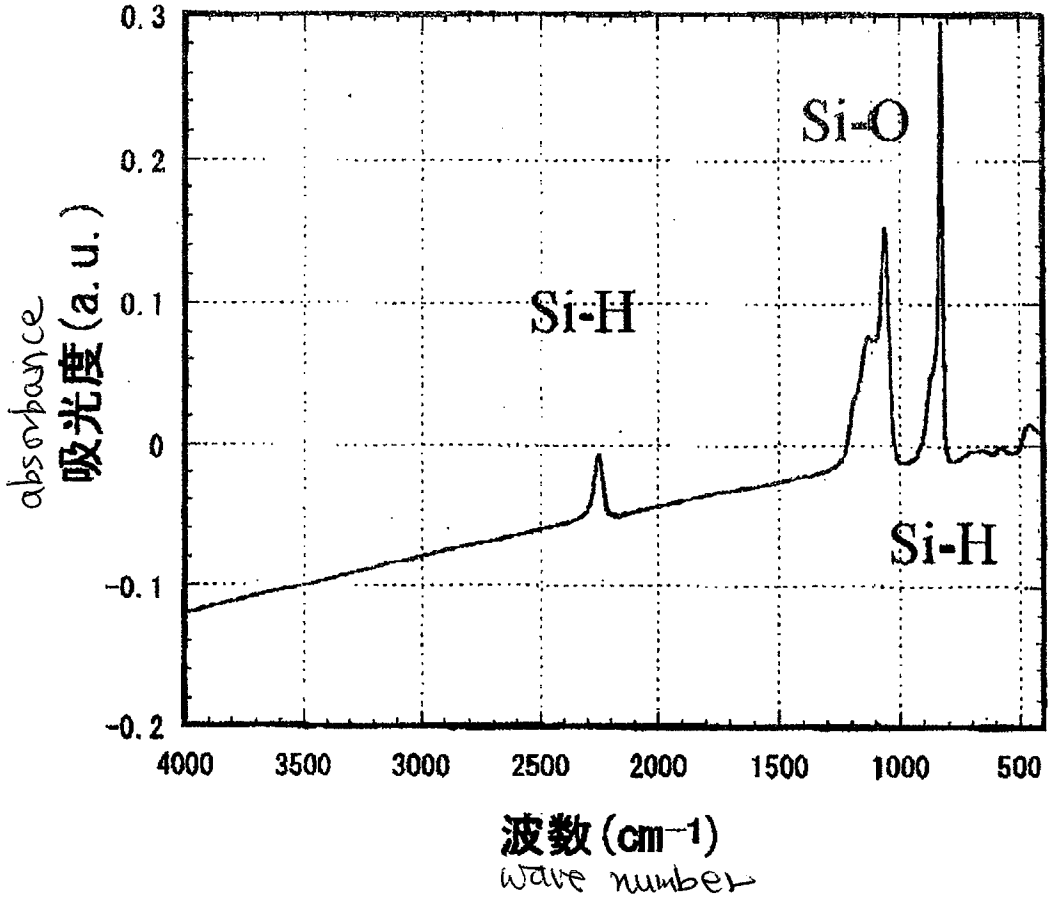
【図１４】Fig.14

dielectric constant	誘電率(@1MHz)	2.9
refractive index	屈折率(@633nm)	1.39
stress	応力(dyne/cm^2)	7.00E+08
hardness	硬度(Gpa)	0.9
shear modulus	弾性率(Gpa)	6
thermal expansion coefficient	熱膨張係数(ppm/deg-C)	18
glass transition temperature	ガラス転位温度(deg-C)	none
thermal conductivity ratio	熱伝導率(W/mk@25 deg-C)	0.31

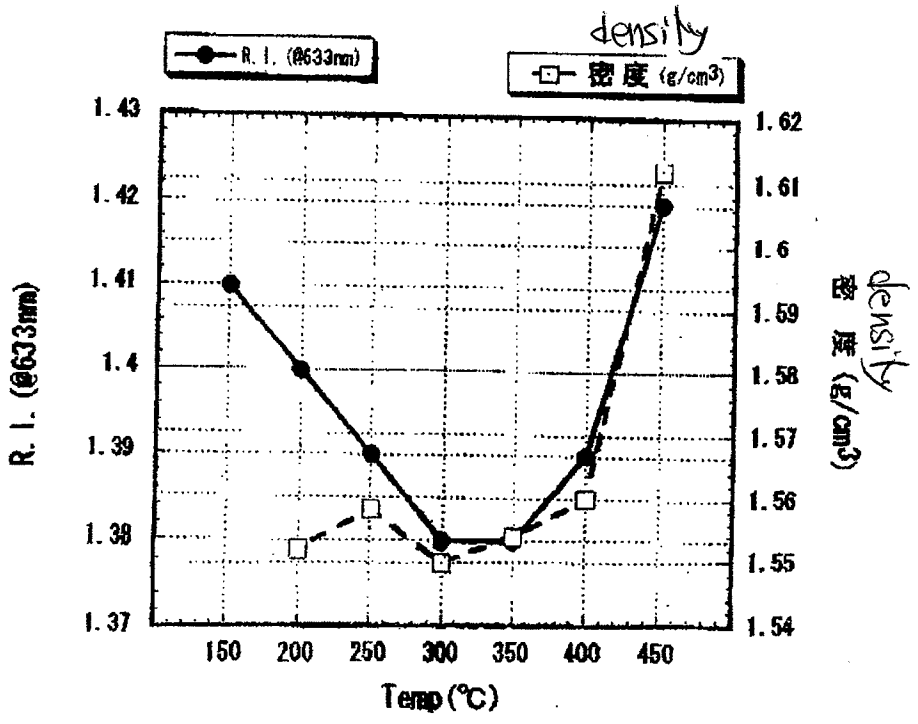
【図１５】Fig.15



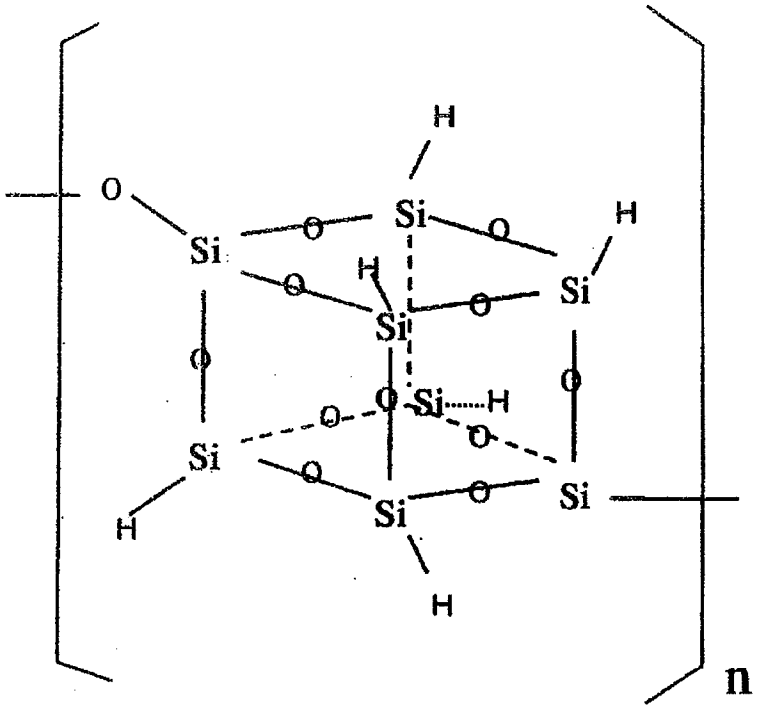
【図１６】 Fig.16



【図１７】 Fig.17

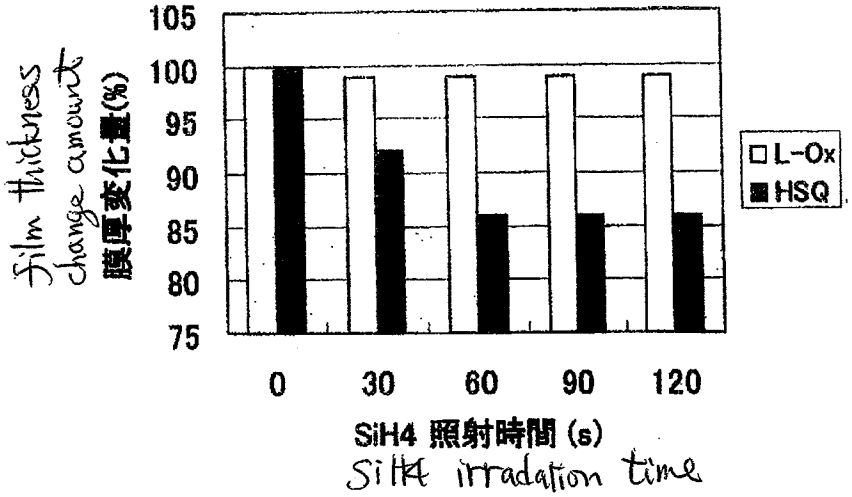


【図１８】 Fig.18

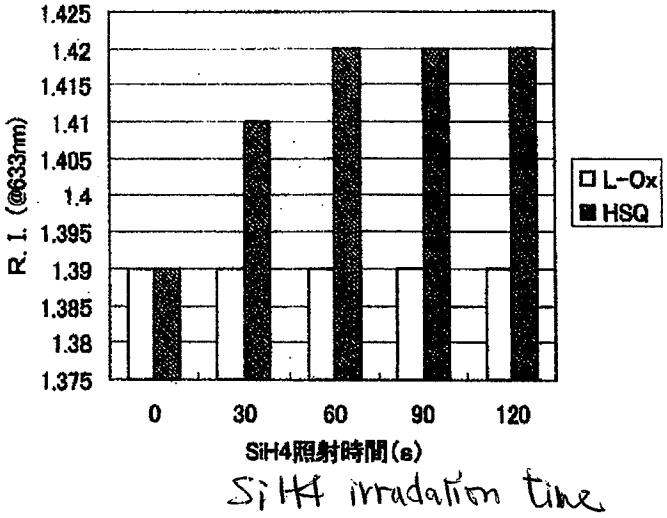


【図１９】Fig.19

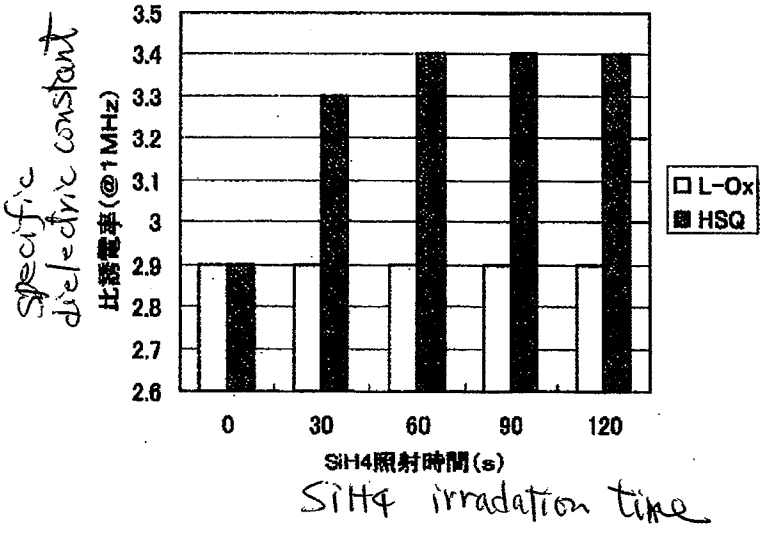
(a)



(b)



(c)



【図２０】 Fig. 20

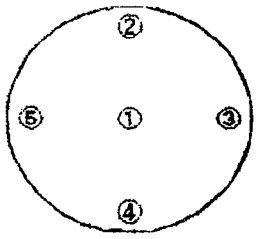
etching rate in case of using LAL 700Å

(a)

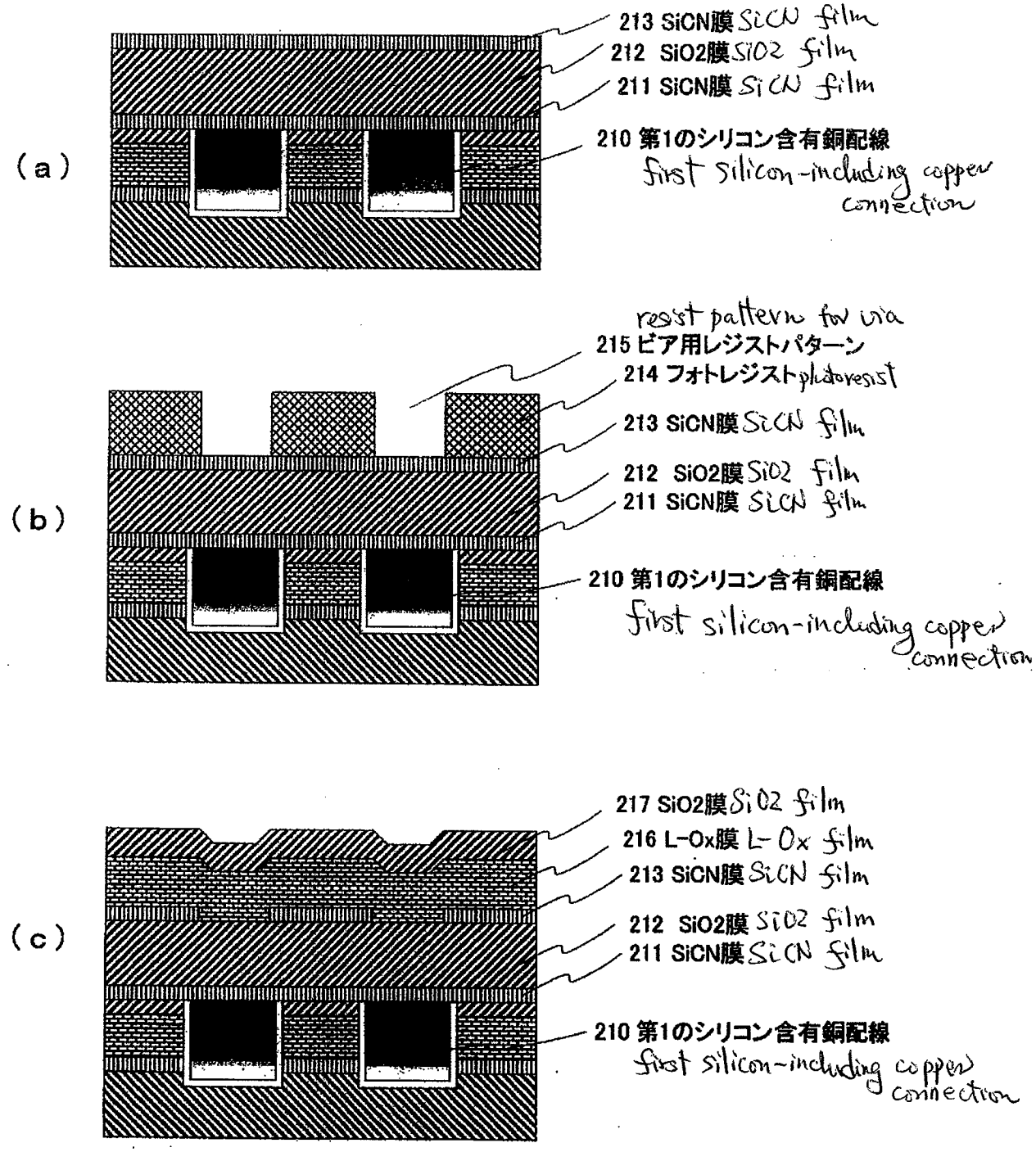
LAL 700Åを用いた場合のエッチングレート

	①	②	③	④	⑤
L-Ox	957	961	915	922	932
HSQ	1198	1232	1007	1101	1058

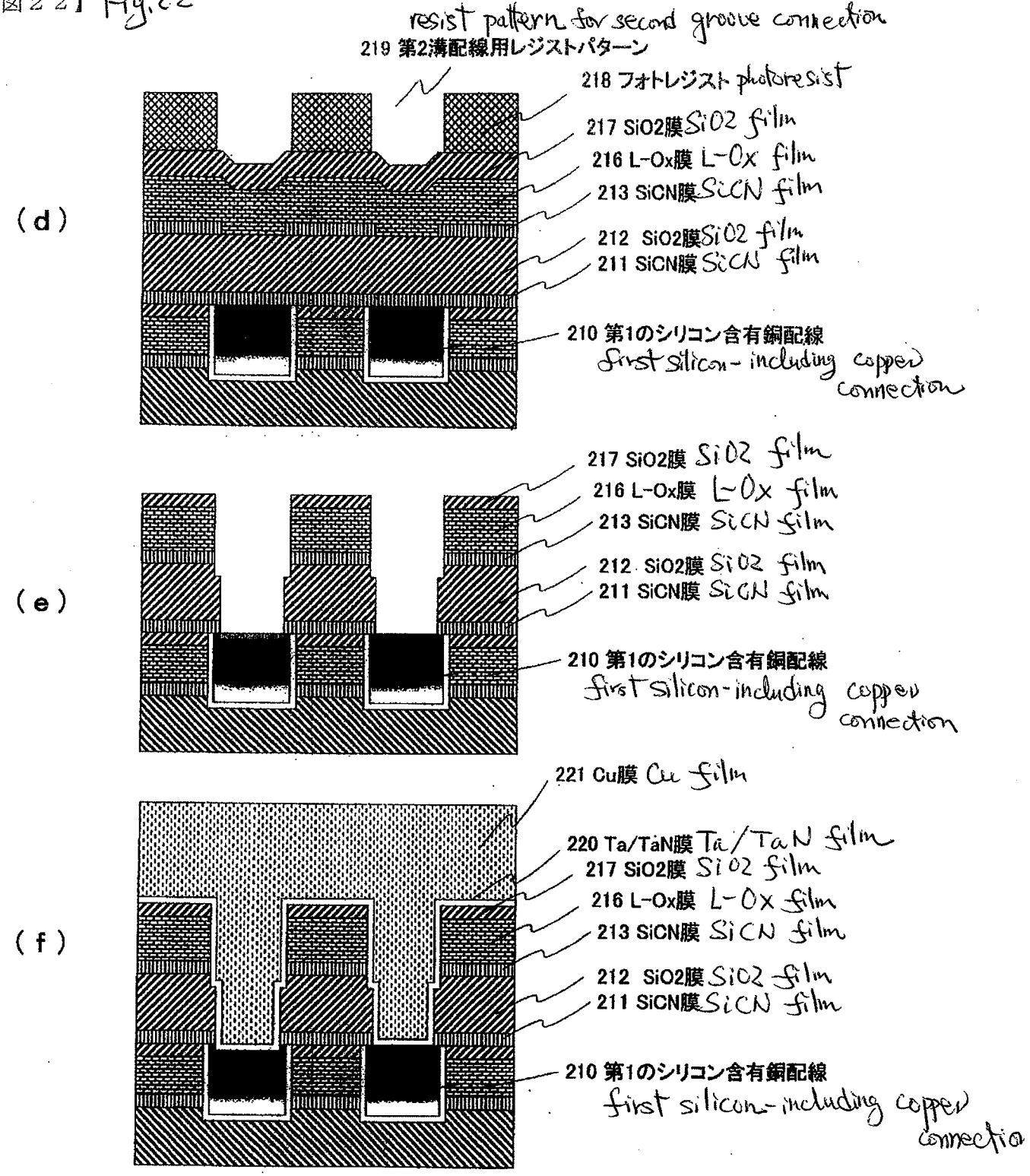
(b)



【図２１】 Fig.21

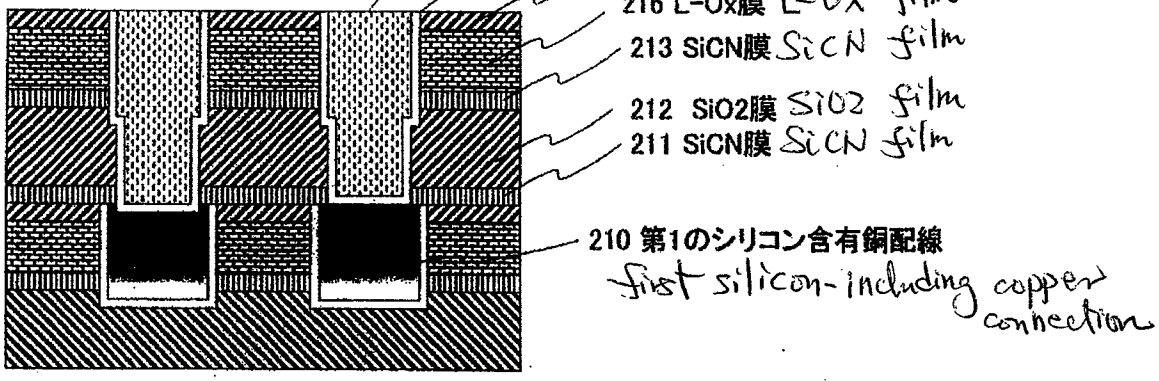

(a)
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(b)
resist pattern for via
215 ビア用レジストパターン
214 フォトレジスト photoresist
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(c)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

【図２２】 Fig.22

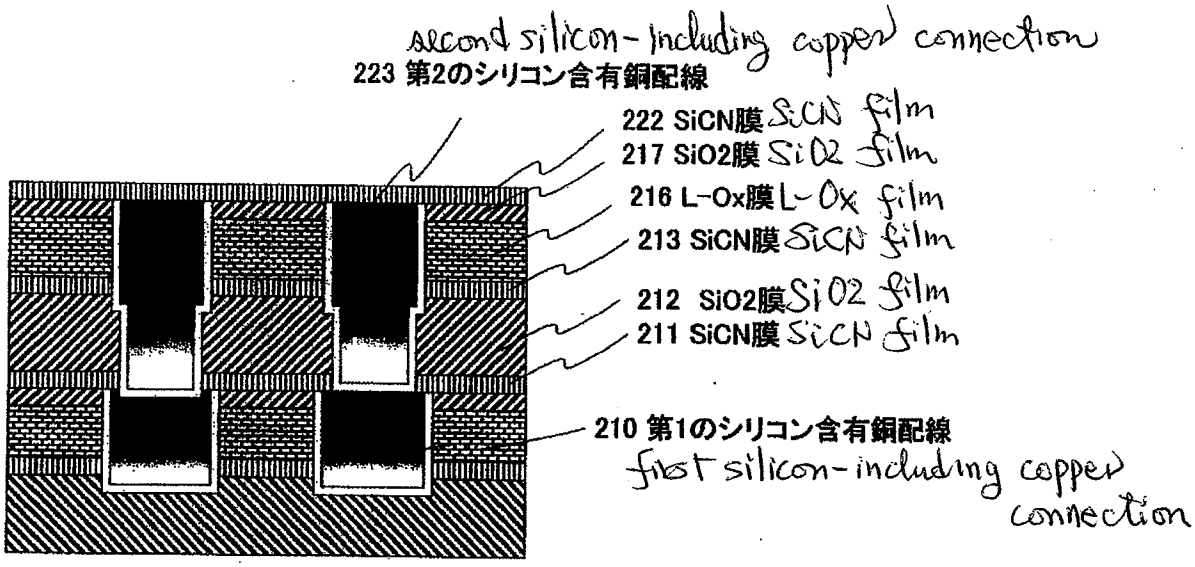

(d)
resist pattern for second groove connection
219 第2溝配線用レジストパターン
218 フォトレジスト photoresist
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(e)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(f)
221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connectio

【図２３】 Fig.23

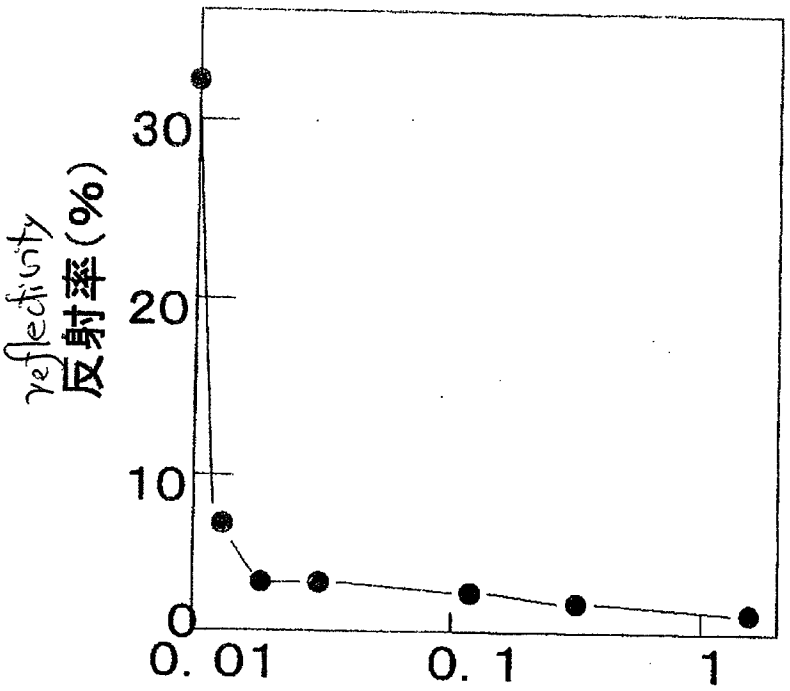
(g)


221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

(h)


second silicon-including copper connection
223 第2のシリコン含有銅配線
222 SiCN膜 SiCN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

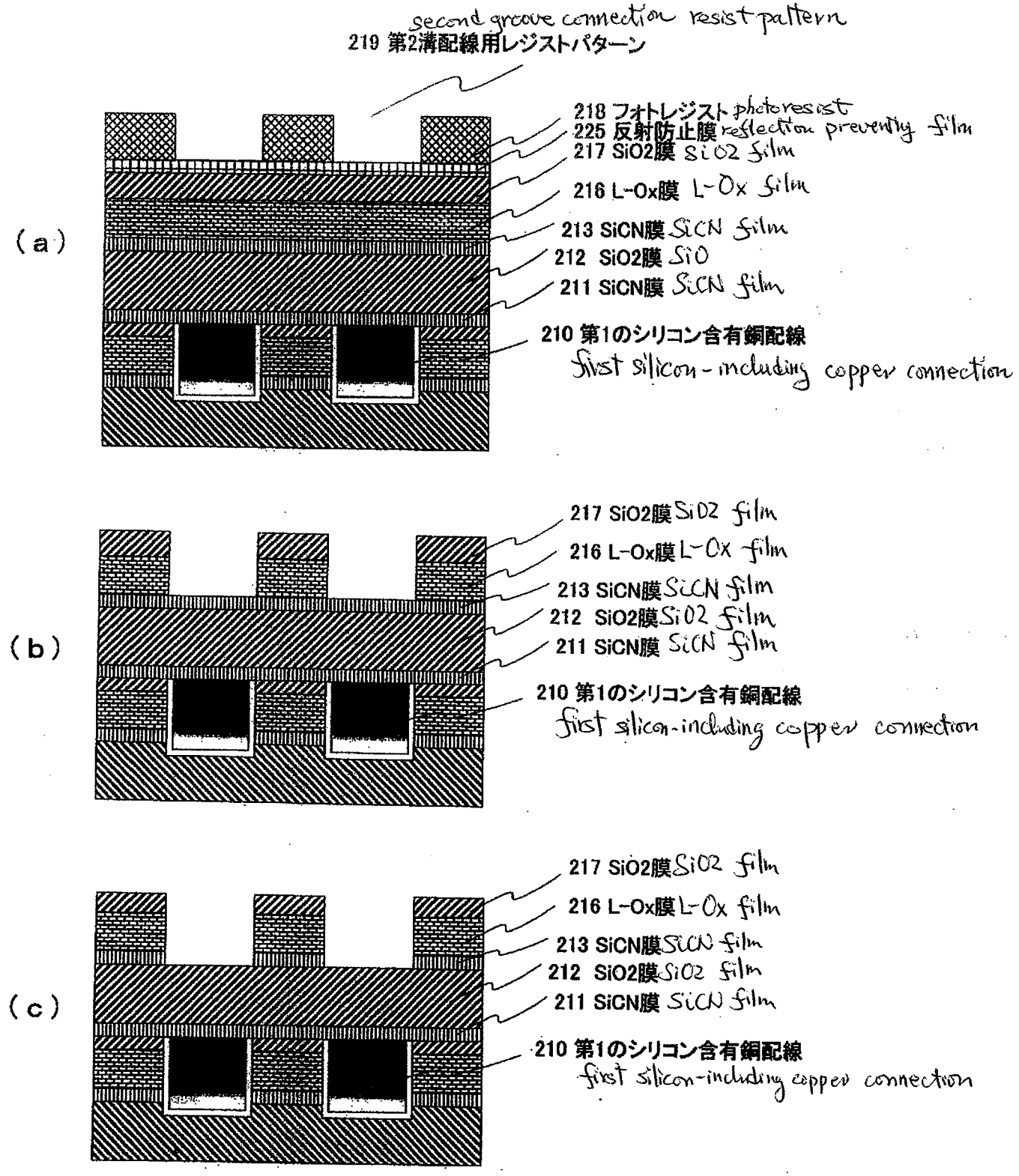
【図２４】Fig.24



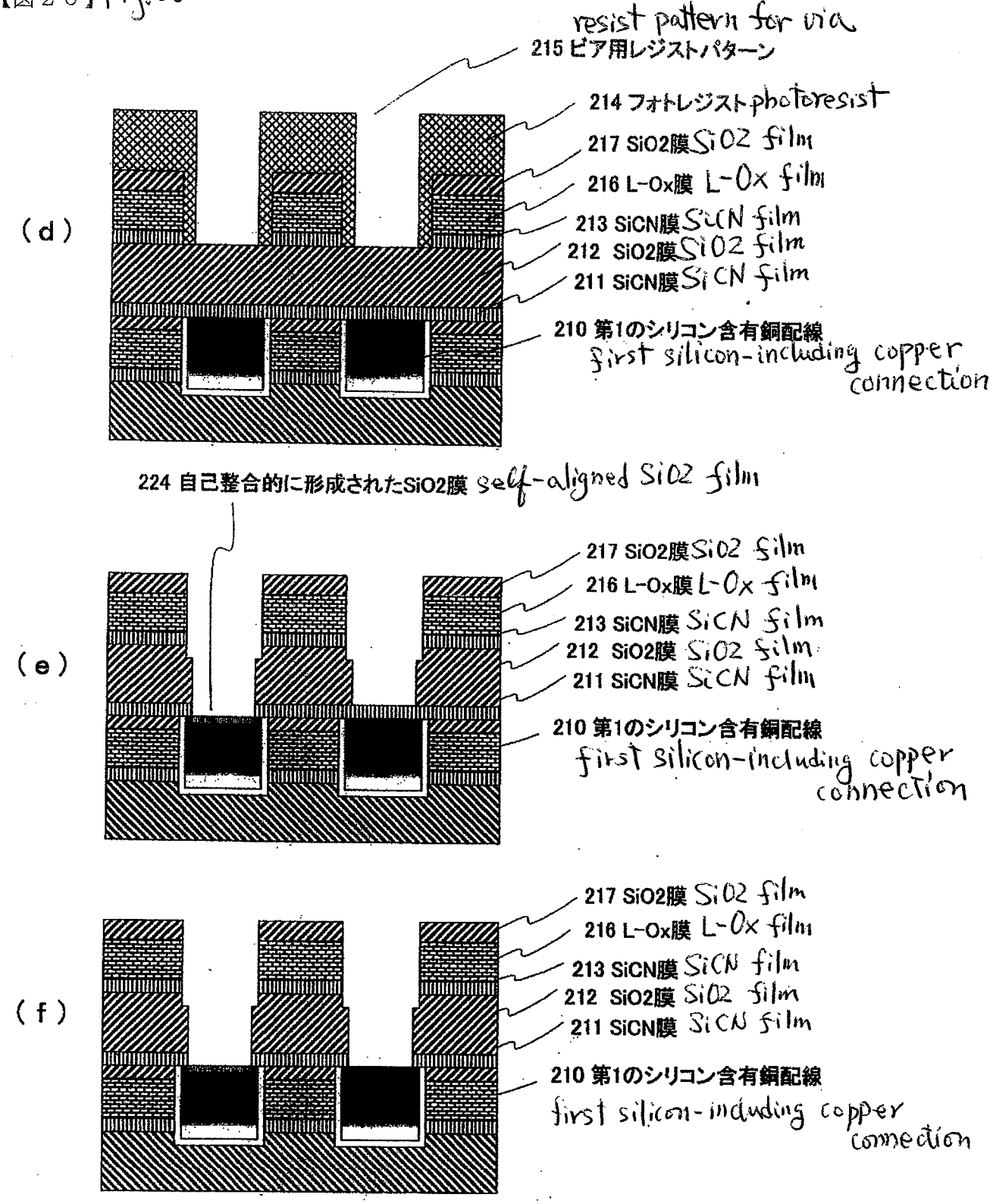
反射率vs シリコン含有率(透過光:100%)

reflectivity vs silicon content (transmitted light: 100%)

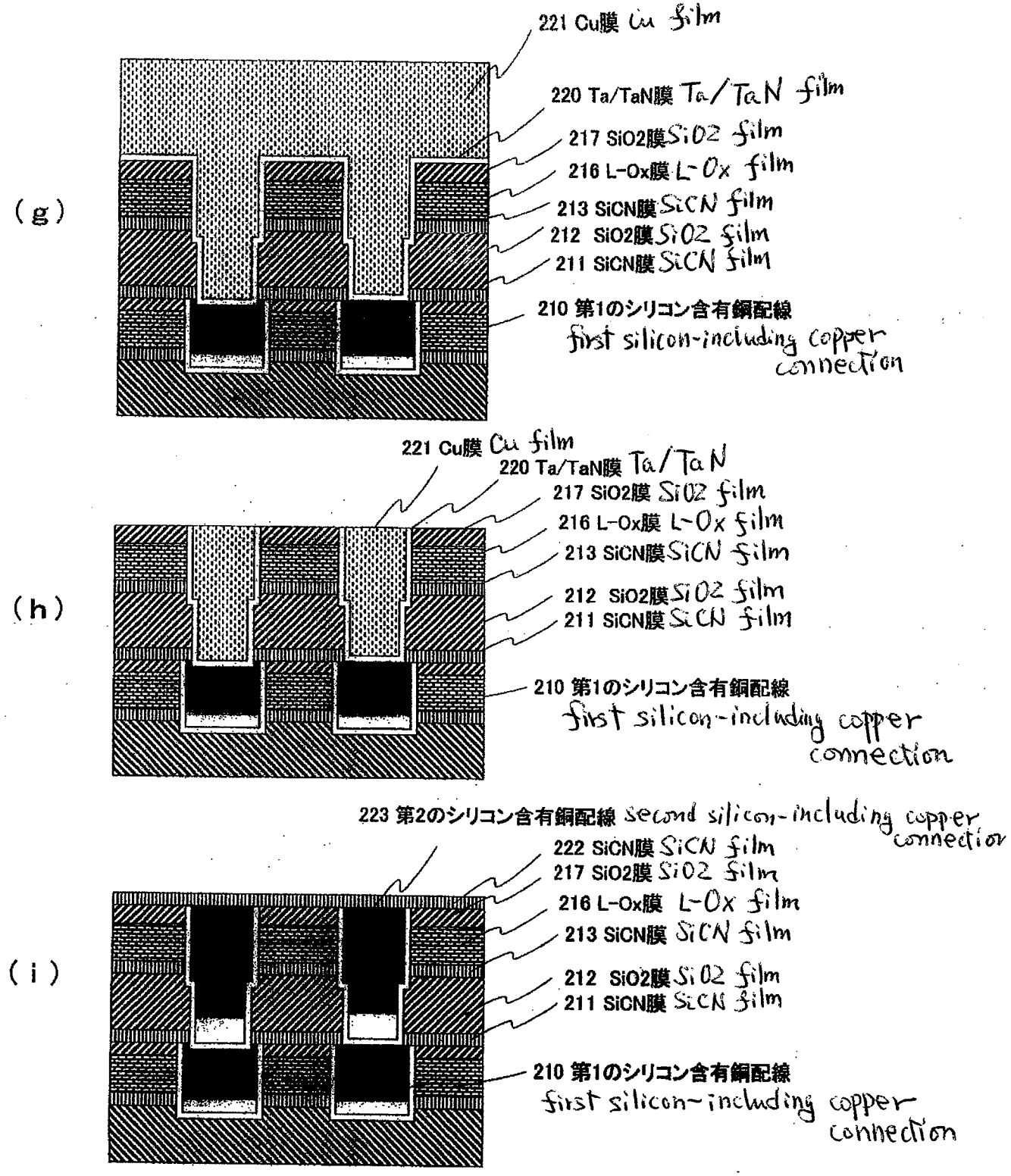
【図２５】


second groove connection resist pattern
219 第2溝配線用レジストパターン
218 フォトレジスト photoresist
225 反射防止膜 reflection preventy film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(a)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(b)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(c)

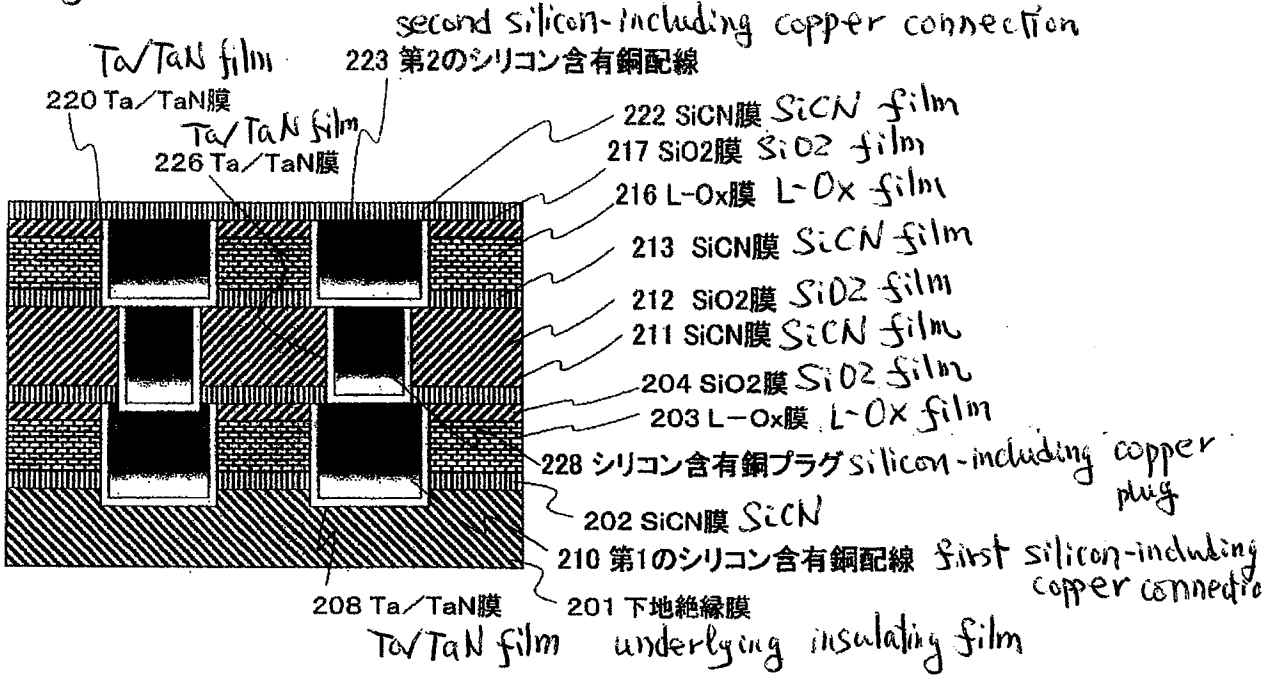
【図２６】Fig.26


(d)
resist pattern for via
215 ビア用レジストパターン
214 フォトレジストphotoresist
217 SiO2膜SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜SiCN film
212 SiO2膜SiO2 film
211 SiCN膜SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
224 自己整合的に形成されたSiO2膜 self-aligned SiO2 film
(e)
217 SiO2膜SiO2 film
216 L-Ox膜L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(f)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

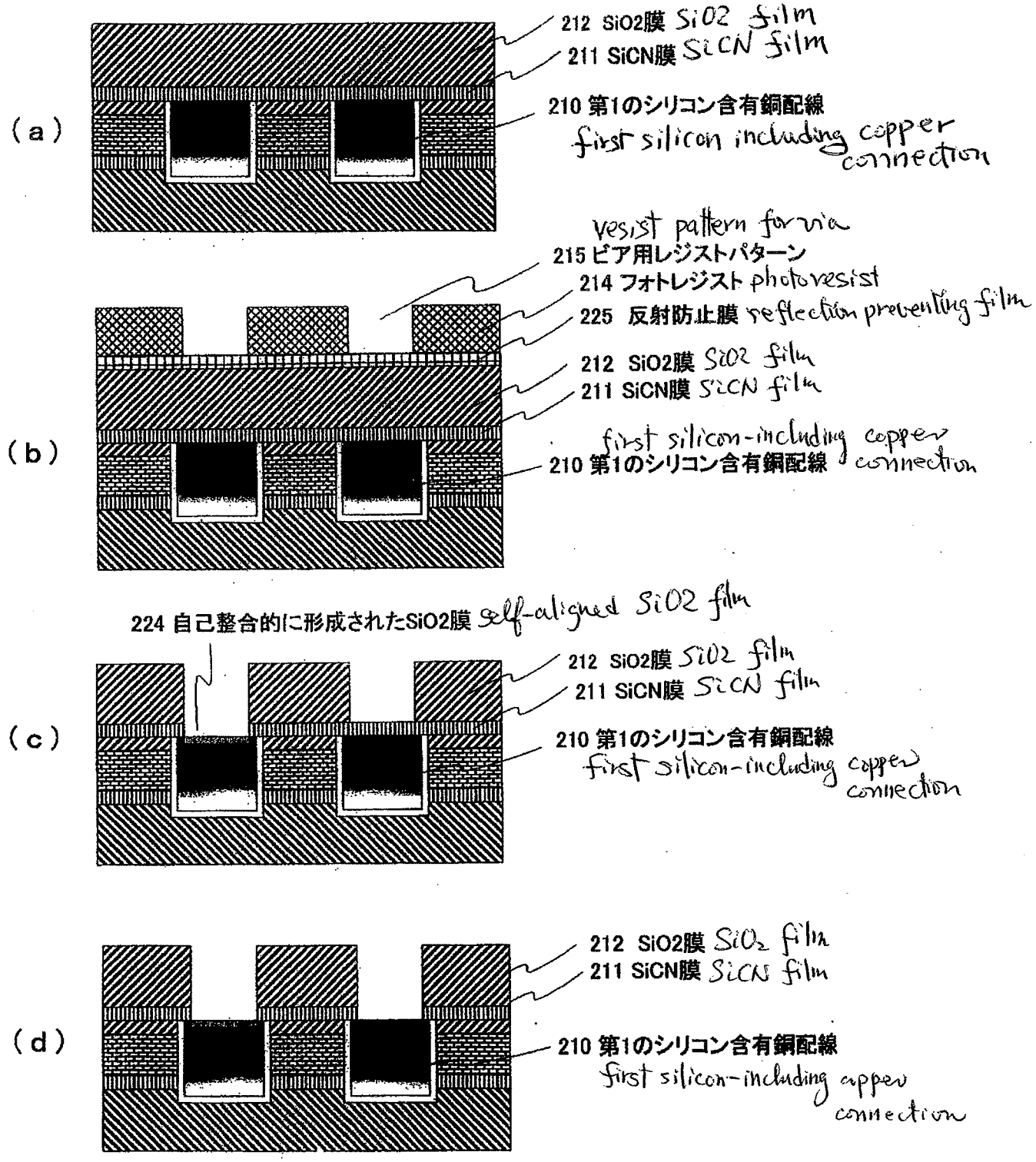
【図２７】Fig.27


(g)
221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(h)
221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(i)
223 第2のシリコン含有銅配線 second silicon-including copper connection
222 SiCN膜 SiCN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

【図２８】Fig.28

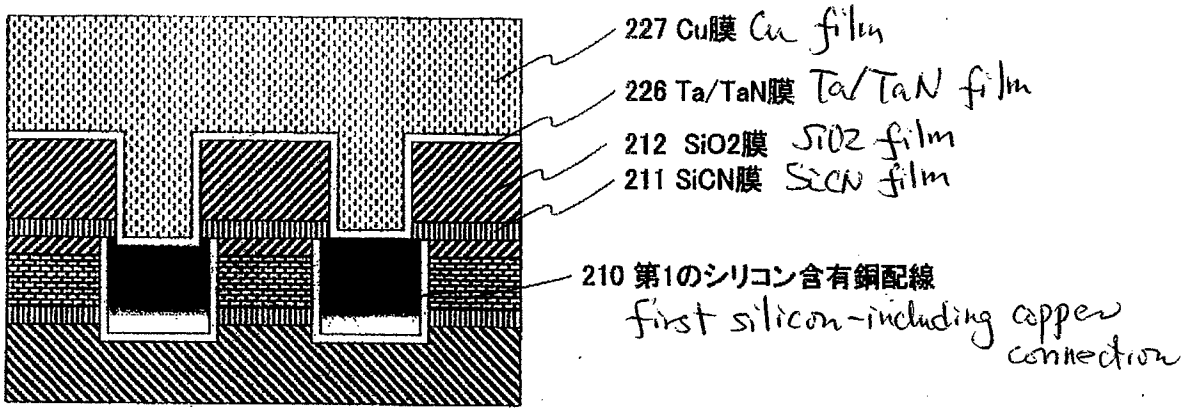

second silicon-including copper connection
Ta/TaN film
223 第2のシリコン含有銅配線
220 Ta／TaN膜
Ta/TaN film
226 Ta／TaN膜
222 SiCN膜 SiCN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
204 SiO2膜 SiO2 film
203 L－Ox膜 L-Ox film
228 シリコン含有銅プラグ silicon-including copper plug
202 SiCN膜 SiCN
210 第1のシリコン含有銅配線 first silicon-including copper connectio
208 Ta／TaN膜
201 下地絶縁膜
Ta/TaN film underlying insulating film

【図２９】 Fig.29

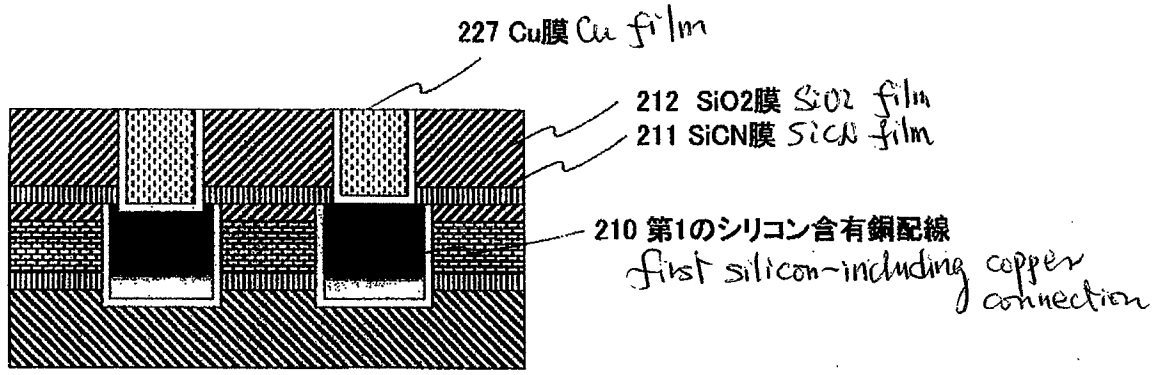

(a)
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon including copper connection
(b)
resist pattern for via
215 ビア用レジストパターン
214 フォトレジスト photoresist
225 反射防止膜 reflection preventing film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
first silicon-including copper connection
210 第1のシリコン含有銅配線
(c)
224 自己整合的に形成されたSiO2膜 self-aligned SiO2 film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(d)
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection

【図３０】Fig.30

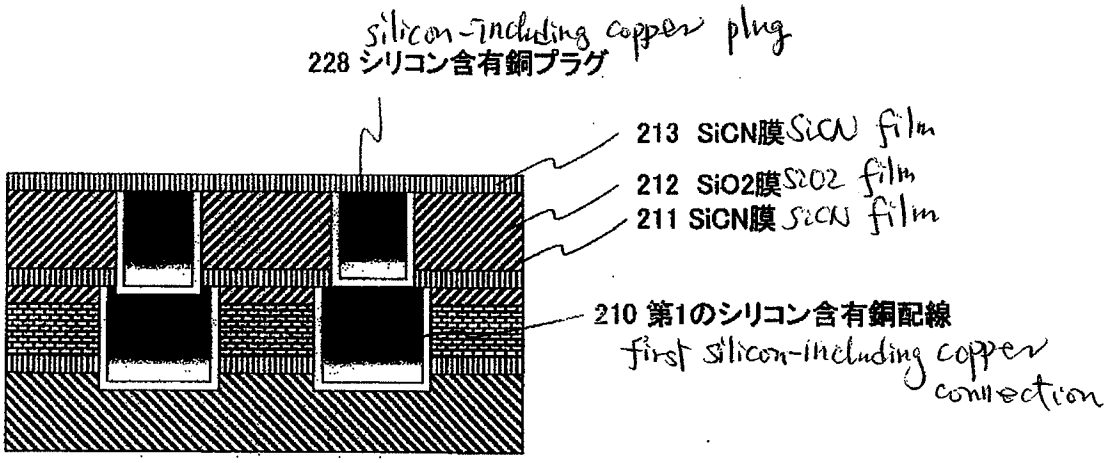
(e)



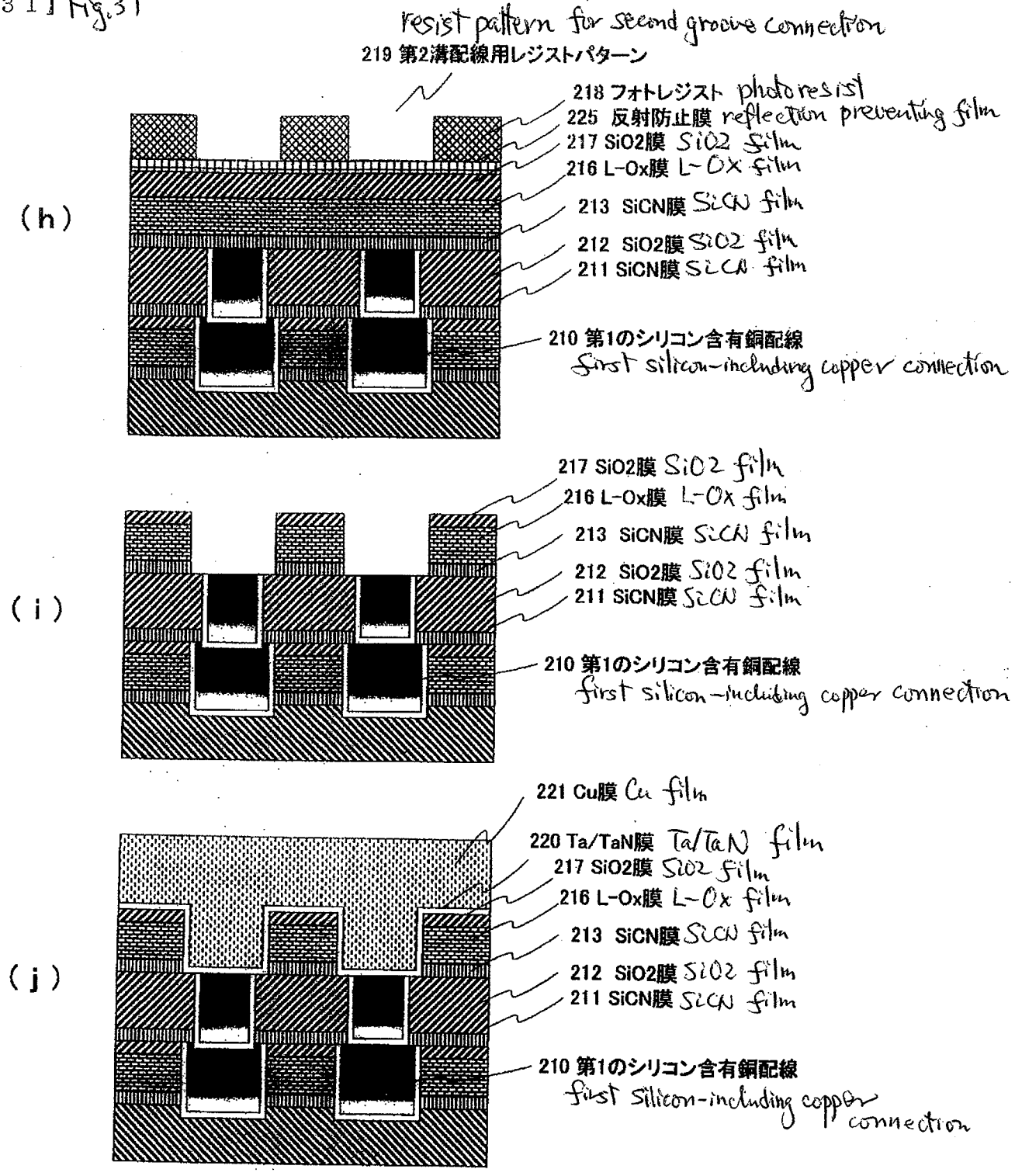
(f)



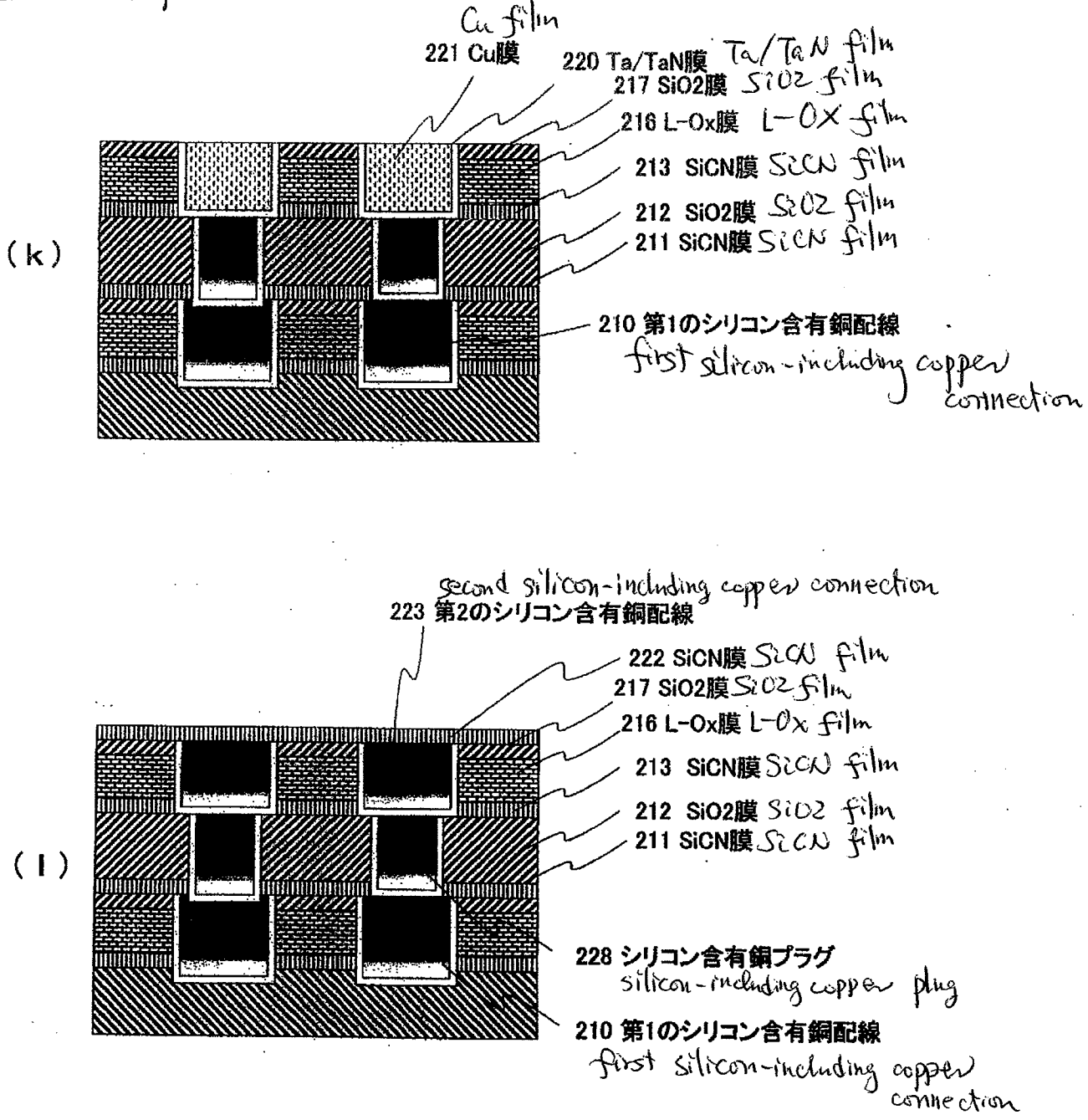
(g)



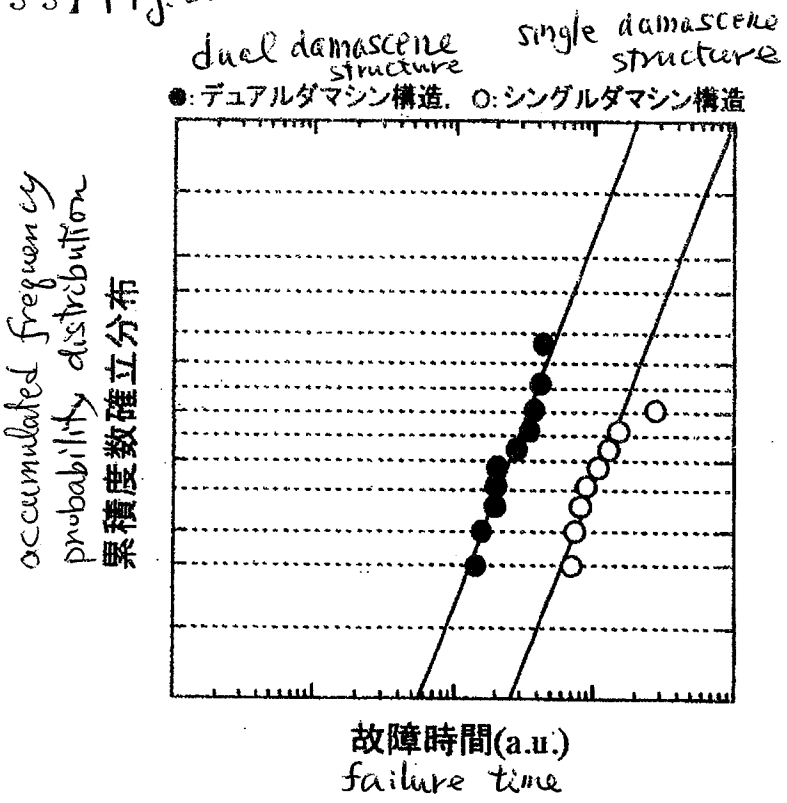
【図３１】 Fig.31


resist pattern for second groove connection
219 第2溝配線用レジストパターン
218 フォトレジスト photoresist
225 反射防止膜 reflection preventing film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(h)
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(i)
221 Cu膜 Cu film
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(j)

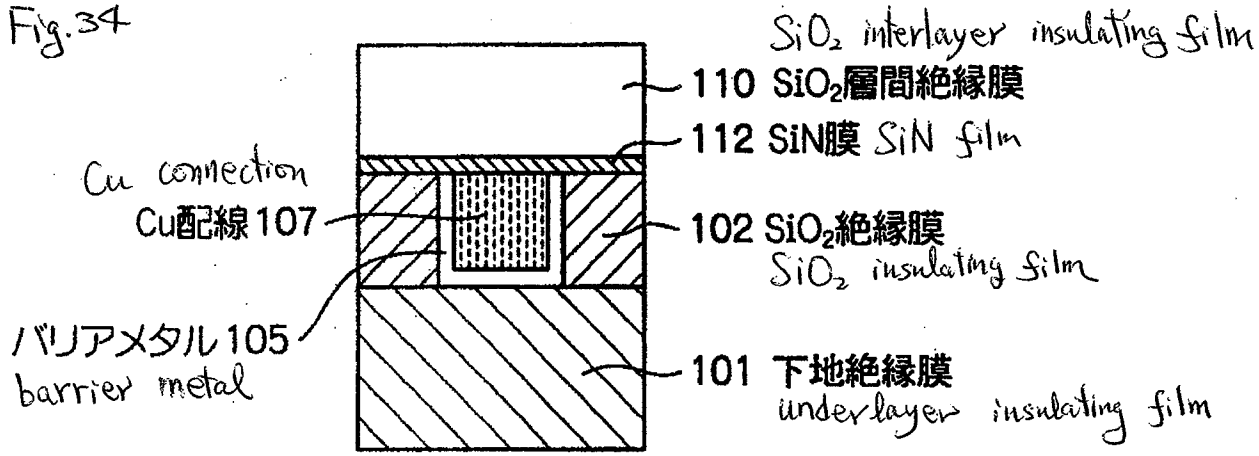
【図３２】 Fig.32


(k)
Cu film
221 Cu膜
220 Ta/TaN膜 Ta/TaN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
210 第1のシリコン含有銅配線
first silicon-including copper connection
(l)
second silicon-including copper connection
223 第2のシリコン含有銅配線
222 SiCN膜 SiCN film
217 SiO2膜 SiO2 film
216 L-Ox膜 L-Ox film
213 SiCN膜 SiCN film
212 SiO2膜 SiO2 film
211 SiCN膜 SiCN film
228 シリコン含有銅プラグ
silicon-including copper plug
210 第1のシリコン含有銅配線
first silicon-including copper connection

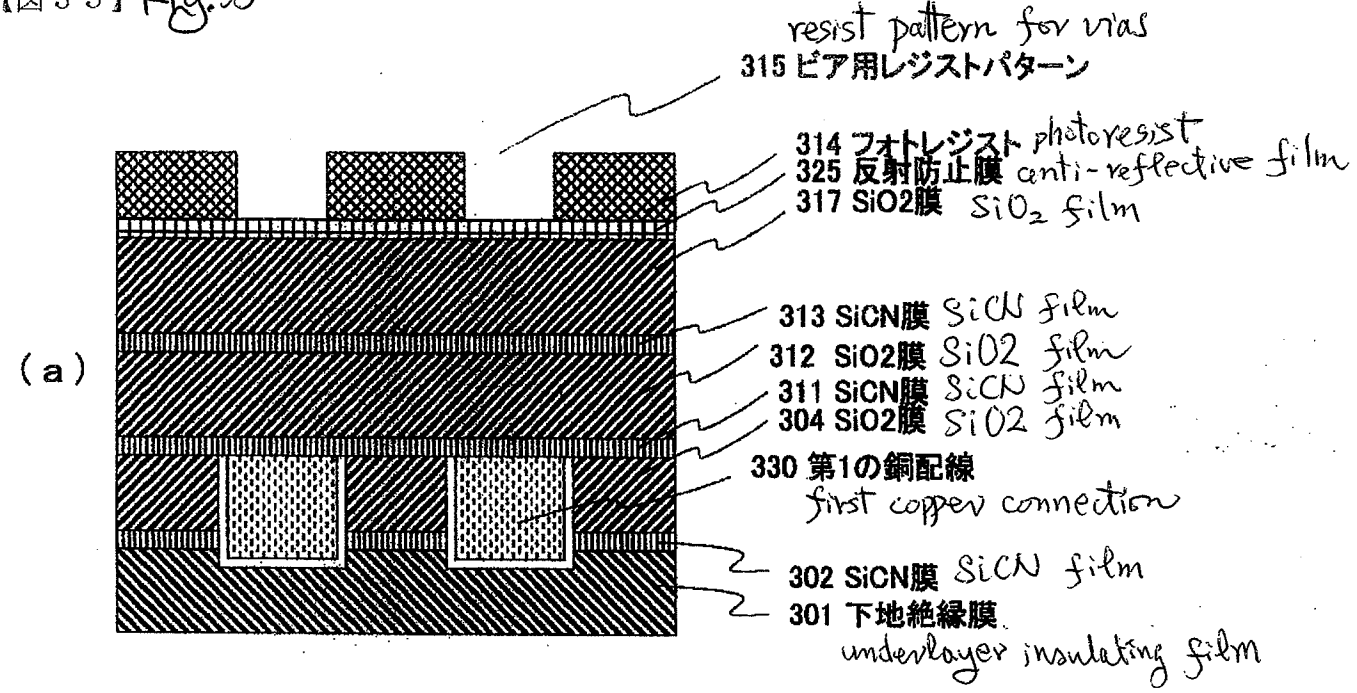
【図３３】 Fig.33

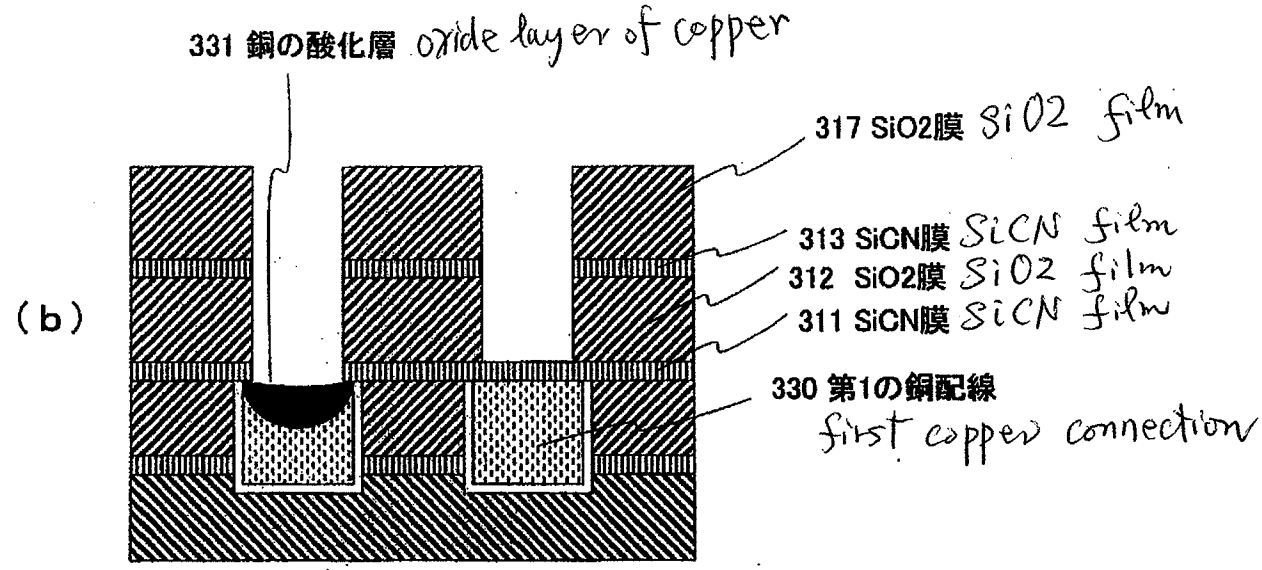


【図３４】
Fig.34

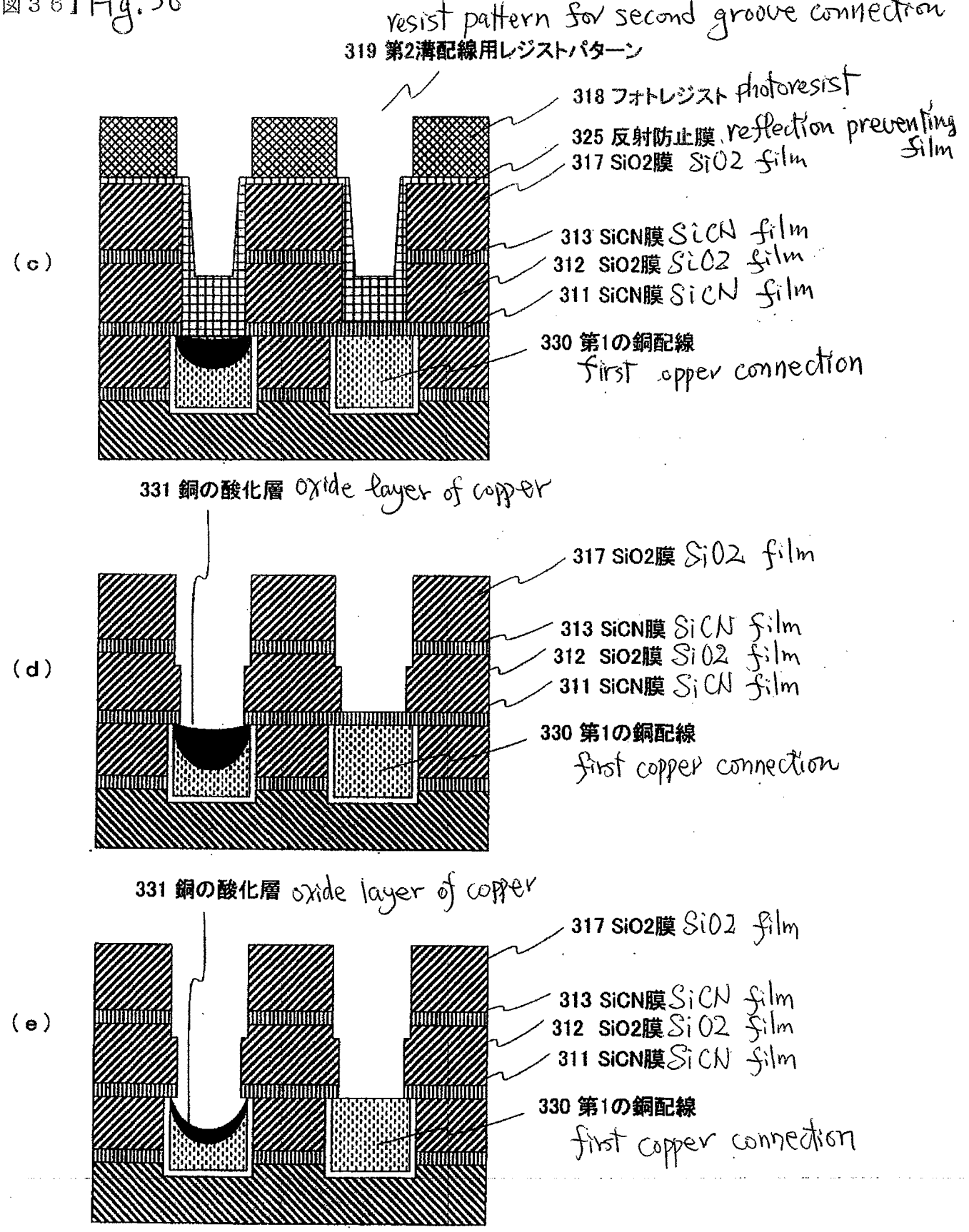


【図３５】 Fig.35

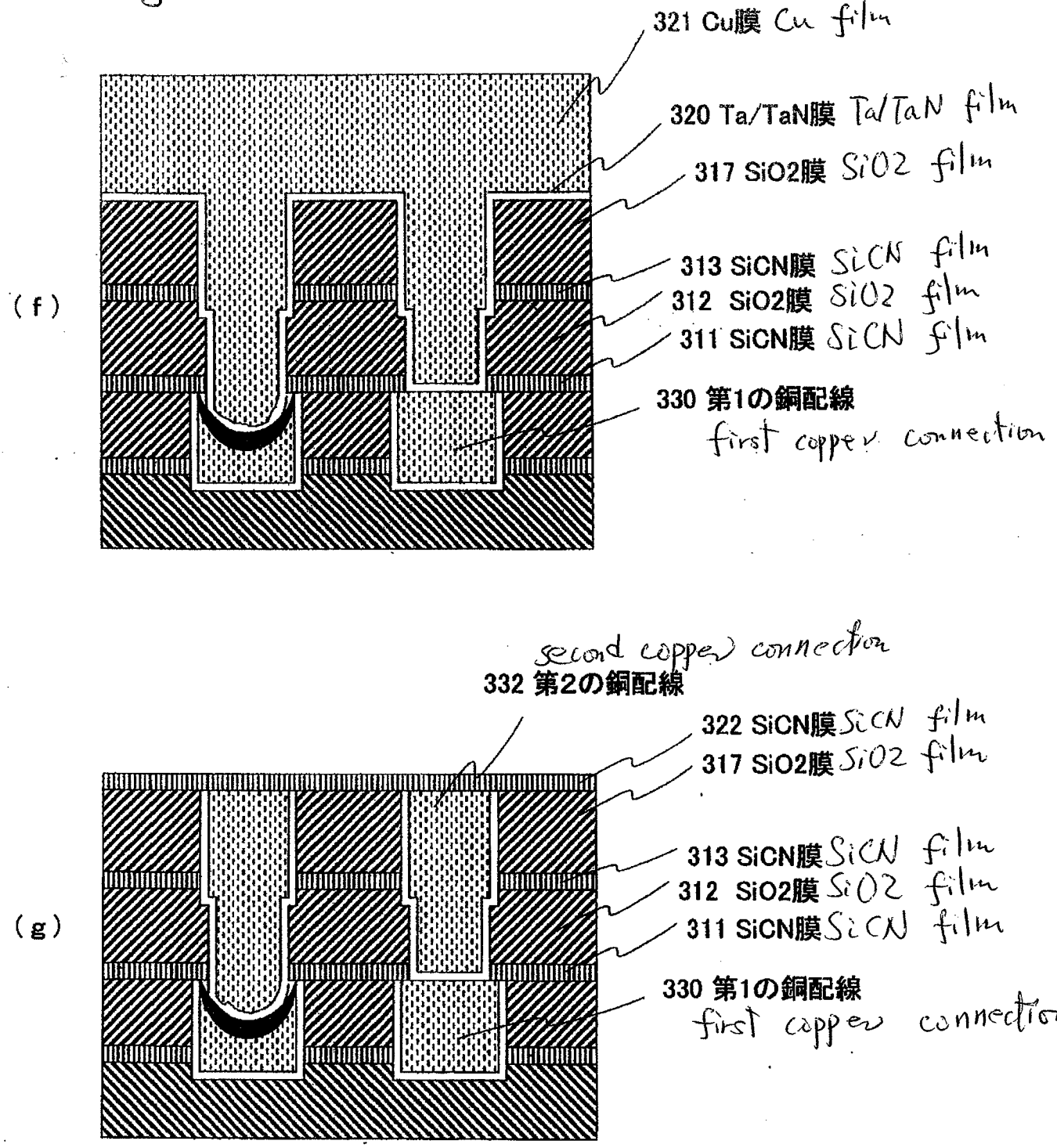

resist pattern for vias
315 ビア用レジストパターン
314 フォトレジスト photoresist
325 反射防止膜 anti-reflective film
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
304 SiO2膜 SiO2 film
330 第1の銅配線
first copper connection
302 SiCN膜 SiCN film
301 下地絶縁膜
underlayer insulating film
(a)


331 銅の酸化層 oxide layer of copper
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection
(b)

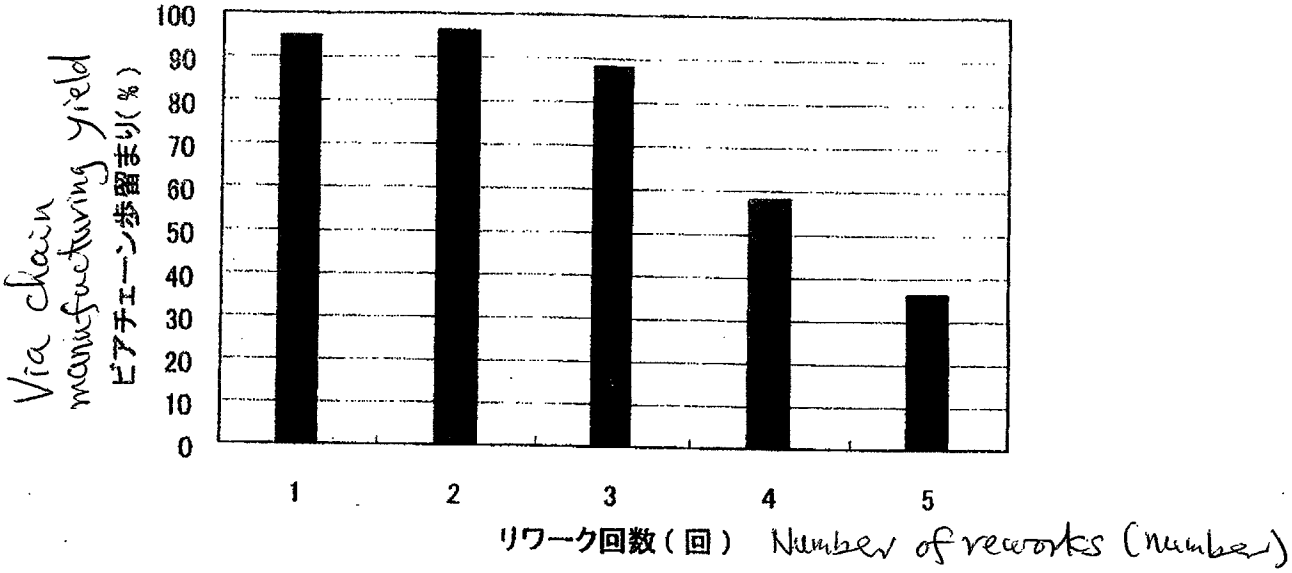
【図３６】Fig.36


resist pattern for second groove connection
319 第2溝配線用レジストパターン
318 フォトレジスト photoresist
325 反射防止膜 reflection preventing film
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection
(c)
331 銅の酸化層 oxide layer of copper
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection
(d)
331 銅の酸化層 oxide layer of copper
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection
(e)

【図３７】 Fig.37


(f)
321 Cu膜 Cu film
320 Ta/TaN膜 Ta/TaN film
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection
(g)
second copper connection
332 第2の銅配線
322 SiCN膜 SiCN film
317 SiO2膜 SiO2 film
313 SiCN膜 SiCN film
312 SiO2膜 SiO2 film
311 SiCN膜 SiCN film
330 第1の銅配線
first copper connection

【図３８】 Fig.38



ビアチェーン歩留まりのリワーク回数依存性 (pure Cu 配線)

Via chain manufacturing yield dependency upon the number of reworks (pure Cu connection)

[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PROBLEM] To provide a manufacturing method of a semiconductor device having a long-life metal connection by improving contact characteristics between a metal connection such as a Cu connection and a metal diffusion preventing film and improving the anti-electromigration characteristics of the metal connection.

[SOLVING MEANS] A metal connection 7 exposing its upper surface is formed in a groove section of an insulating film 2 formed on a semiconductor substrate, and silicon is diffused into the upper surface of the metal connection 7 to form a metal diffusion preventing film 9 on the exposed surface of a silicon-including metal connection 8.

[SELECTED DRAWING] Fig. 3